

Design and Implementation of Content Addressable Memory (CAM) Architecture

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Abstract: Content addressable memory (CAM) is a storage memory with an extra comparison circuitry. It is also called as associative memory, which can be accessed by its own contents instead of addresses in a single clock cycle. Due to access of CAM in a parallel fashion, it has a high speed but consumes very high power. Also, an extra circuitry makes consumption of power higher. In this paper, a CAM architecture based on parity bit is proposed, which will reduce power consumption and increases its performance compared to traditional CAM architecture and other existing designs. Comparison of performance parameters of parity bit based PB-CAM with other existing architectures is presented here and Tanner EDA Tool under 130nm CMOS technology is used for implementation, simulation, and power and delay are estimated for performance evaluation of CAM architectures.

Keywords: CAM, PB-CAM, Associative memory, Parity Bit, MLSA.

1. Introduction

Most memory devices store and retrieve data by accessing its specific memory locations. But content addressable memory (CAM) is a type of memory in which it can be accessed by using its contents instead of using memory locations. As a result, the time required to find an item stored in memory can be reduced. Hence, content addressable memory (CAM) is one such memory that is fast and intuitive.

The fast operation of CAM comes at the cost of increased power consumption and area. The fast operation of CAM is due to the parallel searching operation of contents with all the stored contents in the memory in a single clock cycle. That is, CAM simultaneously searches the input word with all the contents stored in the memory. But, this results in the high power dissipation in the CAM. Hence, due to parallel searching operation in CAM, power consumption is always a major concern while designing CAM.

There are various types of applications in which high speed of operation is required. CAMs can be used in these types of applications. But, the main application of CAM is that it is used in high speed network routers for packet classification and packet forwarding. As CAM applications grow, there is a demand of large CAM sizes which worsens the problem of power. So the main challenge is to reduce power consumption in large capacity CAMs without sacrificing its speed [6].

In this paper, a CAM architecture is proposed in which parity bit is used. This proposed CAM architecture consumes less power and increase the searching speed than the basic CAM. The rest of the paper is organized as follows. Section 2 gives a brief about CAM. Section 3 explains the literature survey done. In Section 4, a parity bit based PBCAM is proposed. Simulation and comparison of results are presented in Section 5. This paper is concluded in Section 6.

2. Content Addressable Memory

Content addressable memory (CAM) is a storage memory in which it can be accessed by using its contents instead of using memory locations [6]. When CAM receives the input data word to search it against table of data words stored in the CAM memory, it returns the address at which the search data word is stored.

2.1 CAM Cell

Content Addressable Memory is a storage device that stores data in its memory cell like usual memory. But additionally it also has a comparison circuitry which is used to compare search data with the data contents stored in its memory simultaneously. This comparison circuitry in the CAM cell occupies extra area than usual memory cell. Hence there is more power dissipation but high speed due to parallel searching operation.

Hence, a basic CAM cell has two functions [1]:

- 1) **Bit Storage** like usual memory RAM. So this bit storage uses simple SRAM cell which contains two cross-coupled inverters forming positive feedback working as a D-latch.
- 2) **Bit Comparison** which is equivalent to XNOR logic operation. It is unique in CAM.

So, it has three modes of operation: *read*, *write* and *compare*.

2.2 Design Concept of CAM

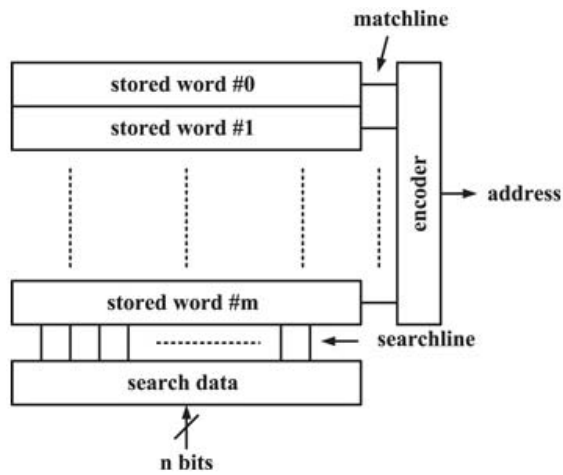


Figure 1: Conceptual View Diagram of CAM

The conceptual view diagram of CAM is shown in Figure 1. It shows that CAM contains m data words in which data is stored. The search word is the n bit input data which is broadcasted onto the search lines to compare it with the table of stored words simultaneously [6]. There is a matchline associated with each stored word which indicates whether the search data is matched with the stored data or not. If the search data is matched with stored data, it is a match case otherwise mismatch case. These matchlines are fed to an encoder. This encoder generates the binary location corresponding to matchline which indicates the match case. If there are more than one matchline that indicates the match case then the priority encoder can be used to generate the matched memory location. The priority encoder gives the matching address location corresponding to highest priority matchline.

3. Literature Review

In [9], a technique was proposed to reduce power consumption of matchlines in content addressable memories (CAMs) called *selective precharge technique*. In selective precharge technique, the matchline is divided into two segments. Firstly, the searching operation is performed in the first segment in which first few bits of a word i.e. a small subset of CAM cells are searched. If there is a matching of data in the first segment only then searching of remaining bits in the second segment will be activated. In [8], an architecture was proposed having low-power, low-cost, and high-reliability features called as *fully parallel precomputation-based content addressable memory (PB-CAM)*. This design is based on a precomputation skill that saves power consumption of the CAM by reducing number of comparisons in the second part of the comparison process. In this design, *one's count approach* is used for precomputation. Hence, a *one's count parameter extractor* was designed using a chain of full adders but it increases delay as data bit length increases. In [7], a technique was proposed to reduce power consumption of matchlines in content addressable memories (CAMs) called *pipelining technique*. In this technique, the search operation is pipelined by breaking the match-lines into many segments. Since most stored words do not match in their first segments, the search operation is aborted for subsequent segments. Hence, power

gets reduced. The power savings of the pipelined MLs is a result of activating only a small portion of the matchline segments. In [5], a new approach for PBCAM known as a *Block-XOR approach* was proposed to improve the efficiency of low power precomputation-based CAM (PB-CAM) proposed in [8]. In this paper, a *Block-XOR parameter extractor* for low power PB-CAM was proposed. This paper presented theoretical and practical proofs to verify that this proposed Block-XOR PB-CAM can effectively achieve greater power reduction by reducing the number of comparison operations in the second part of the comparison process. This implies that this approach is more flexible and adaptive for general designs. In addition, the proposed Block-XOR PB-CAM can compute parameter bits in parallel with only three XOR gate delays for any input bit length (constant delay of search operation).

4. Proposed Work

In this proposed approach, parity bit is introduced as parameter for comparison operations. The parity bit generator is a parameter extractor here that will be used for generating parity bit value. The advantage of using parity as a parameter is that parameter memory is highly reduced in comparison with existing PBCAM as only one bit i.e. $k=1$ is required for storing parameter corresponding to each stored word whatever may be the length of input data bits. Hence, the number of comparison operations in pre-computation is highly reduced and hence the power consumption of parameter memory. So, overall power consumption of the CAM is reduced. Compared with existing PBCAM, the proposed architecture has improvement in complexity and area but in comparison with traditional PBCAM, it has little area overhead. The searching speed is also increased due to reduction in complexity and reduction in parameter comparison operations. By using parity bits, delay for each search operation is reduced. Hence, it boosts the search speed of parallel CAM.

4.1 Parity Bit

The number of bits having logic value „1“ in a given binary data is counted. If number of bits in the binary data is odd, then the parity bit value is „1“ and if the number of one's in a binary data is even, then the parity bit value is „0“.

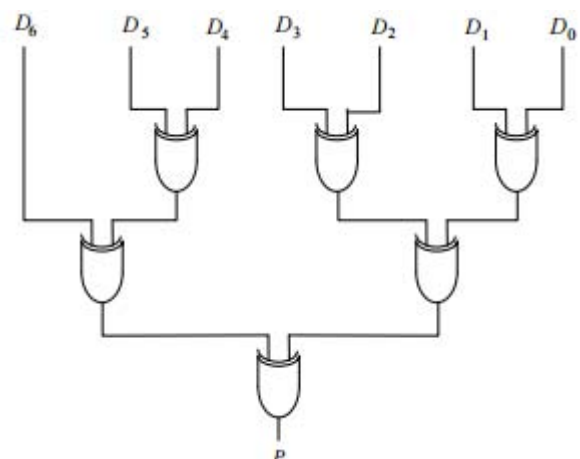


Figure 2: Logic Circuit of Parity Bit Parameter Extractor.

4.2 Proposed PBCAM Architecture

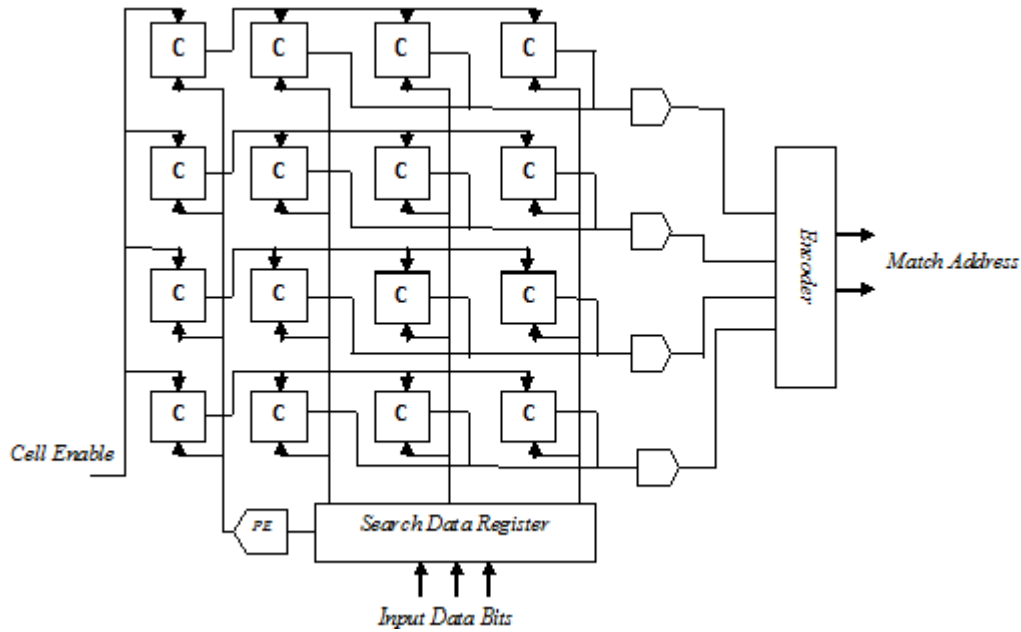


Figure 3: Parity based PBCAM Architecture

Like existing PBCAM, in this design also, first the parity bit is extracted using parity bit generator and comparisons of extracted parity bit is made with that of stored parity bits. Then, according to the results of parity bit comparisons, comparisons in data memory takes place. Comparisons in data memory will be made only with those stored data words whose corresponding parity bit will be matched with that of input word's parity bit.

5. Simulation Results

The proposed design is implemented and simulated using Tanner Tool under 130nm process environment. Figure 4 shows the simulation waveform of proposed design and Table 1 compares power and delay of various CAM architectures.



Figure 4: Simulation Waveform of Proposed Parity Bit based PBCAM.

It is clear from the below table that proposed design of PBCAM consumes less power and delay than the existing designs.

Table 1: Result Comparisons

Parameters	One's Count PBCAM [3]	Block-XOR PBCAM [3]	Conventional CAM	Proposed PBCAM
Technology	0.35 μm	0.35 μm	0.13 μm	0.13 μm
Power (mW)	266.84	146.48	61.02	33.24
Delay (ns)	25	15	2.18	1.18

6. Conclusion

A parity based pre-computation based content addressable memory (PB-CAM) has been proposed in which parity bit is used as a parameter. In the traditional CAM, a large number of comparisons are there for accessing the CAM. So, there is a large amount of power consumption. By proposed design, the number of comparisons in the data memory has been reduced for accessing the CAM than the traditional CAM by little area overhead. Therefore, the proposed design significantly saves power and provides high performance than the traditional CAM. Moreover, parameter memory required for storing parameters and hence parameter memory comparisons have been reduced than existing PBCAMs. So, parameter comparison power and parameter memory area are also reduced than existing PBCAMs (One's Count and Block-XOR), making it efficient to implement and use practically. The proposed design has been implemented using Tanner EDA Tool under 130nm technology. Simulation results are showing that our proposed design achieves less power and high performance with 33.24mW and 1.18ns respectively than the traditional CAM with 61.02mW and 2.18ns. In the future, we can reduce more power as compared to that of proposed design. Work can also be done on reducing the area of CAM.

References

- [1] Dejan Georgiev, "Low Power Concept for Content Addressable Memory (CAM) Chip Design," International Journal of Advanced Research in

Electrical, Electronics and Instrumentation Engineering,
Vol.2, Issue 7, July 2013.

- [2] S. Jeeva, S. Bharathi and Dr. C. N. Marimuthu, "Low Power Architecture of Banked Pre-Computation Based Content Addressable Memory", International Conference on Computing, Communication and Information Technology (ICCCIT 2012), p.p. 156-160, June 2012.
- [3] Rafeekha M. J, V. Lakshmi Narasimhan, "Banked Approach of Low Power Design of Pre-Computation Based Content Addressable Memory", International Journal of Modern Engineering Research (IJMER), Vol. 2, Issue 3, p.p. 1424-1429, May-June 2012.
- [4] Subha. M, "The Efficient Architecture Methods for Low Power Content Addressable Memory- Survey", Recent Advances in Networking, VLSI and Signal Processing, p.p. 141-146.
- [5] S. J. Ruan, C.Y. Wu, J. Y. Hsieh, "Low power design of pre-computation based content-addressable memory," IEEE Transactions Very Large Scale Integration (VLSI) Systems, Vol. 16, No. 3, p.p. 331-335, March 2008.
- [6] K. Pagiamtzis and A. Sheikholeslami, "Content-Addressable Memory (CAM) Circuits and Architectures: A Tutorial and Survey," IEEE Journal of Solid-State Circuits, Vol. 41, p.p. 712-727, March 2006.
- [7] K. Pagiamtzis and A. Sheikholeslami, "A low-power content-addressable memory (CAM) using pipelined hierarchical search scheme," IEEE J. Solid-State Circuits, Vol. 39, No. 9, p.p. 1512-1519, Sep. 2004.
- [8] C.-S. Lin, J.-C. Chang, and B.-D. Liu, "A low-power precomputation-based fully parallel content-addressable memory," IEEE J. Solid-State Circuits, Vol. 38, No. 4, p.p. 654-662, Apr. 2003.
- [9] C. A. Zukowski and S.-Y. Wang, "Use of selective precharge for low power content-addressable memories," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), Vol. 3, p.p. 1788-1791, 1997.