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Improved Power Reduction and Aging Mitigation Using Gate Replacement and Voltage Scaling Techniques

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Abstract: ***As the VLSI technology and supply/threshold voltage continues scaling down, power consumption and aging are the major problems affecting circuit performance. The aging effect in circuits is due to the Negative Bias Temperature Instability (NBTI) which is a well-known reliability concern for PMOS transistors caused by the negatively biased gate voltages at high temperatures. In the meantime, reducing power consumption and aging optimization remains to be main design goals for almost all circuits. Major power dissipation is contributed by static as well as dynamic power. Static power is mainly deals with leakage power, which can be reduced by Gate replacement algorithms, which is one of the important standby mode internal node control technique. At the same time, aging effects are also optimized by this technique. In the other side, dynamic power consumption can be minimized by adopting multilevel voltage scaling technique. Applying a voltage scaling technique that changes the supply voltage of gates to a lower value in CMOS circuits is an effective way of reducing power consumption. In addition, this proposed method will compare with the existing power reduction techniques. Experimental results show that this method can effectively reduce the static, dynamic power leakages and circuit delay compared to previous techniques***.

Keywords: negative bias temperature instability (NBTI), gate replacement, aging, voltage scaling

1. Introduction

Power dissipation has one of the important design parameter in CMOS technology due to decrease in feature size, which results the increase in chip density and operating frequency. With increasing demand of System On Chip (SOC), more and more transistors are getting added in modern VLSI chip corporate new architectural features leading to the risk of very high power dissipation in a die. On other hand, now a days customers look for portable handheld devices like smart phones, tablet PC having high battery lifetime. Therefore low power dissipation by VLSI circuits has become a key design parameter. Considering energy crisis being the major problem in modern design manufactures which cannot afford to allow excessive power leakage from a single chip. More power dissipation leads to heat up the devices thereby reducing the performance, reliability and durability also. Hence, the need for low power VLSI circuits techniques arises. The world now need ways to efficiently reduces the dissipation of huge amount of power from the circuits while keeping pace with ever increasing demands of more and more features in a single die. High power consumption also increases the current density in the supply lines, causing greater electro migration problems. This also impacts battery powered portable devices by requiring either large battery packs or unacceptably short operating time.

For any circuit, total power can be calculated as the sum of static power as well as the dynamic power. Hence, total power consumption is contributed by static power as well as dynamic power dissipations. Static power is consumed even when a chip is not switching and which mainly occurs due to leakage current. Prior to the 90 nm node, leakage power was the primary concern during sleep mode because it was negligible compared to dynamic power dissipation. Leakage can account for as much as a third of total active power in nanometer processes with low threshold voltages and thin gate oxides Sub threshold leakage is usually the dominant source of static power. Also, gate leakage, junction leakage and punch through leakage leads to static power consumption.

Dynamic power depends on activity factor, capacitance, voltage and frequency that consist mostly of the switching power. Since most gates do not operate/switch at every clock cycle, they are often accompanied by a factor, called the activity factor. The switching power depends on the sum of the effective capacitances of all the nodes. A CMOS circuit dissipates more power by charging the various load capacitances whenever they are switching. This is also caused by short-circuit power dissipation which occurs on both pull up and pull down networks are partially ON while the input switches. It increases as the input edge rates become slower because both networks are ON for more time.

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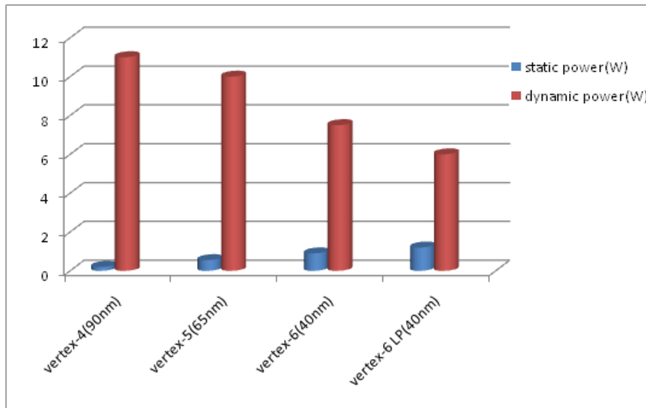

Figure 1: Technology influence on total Power

In figure1, the results shows the total power dissipation of the same logic design with various technology properties and supply voltage variations obviously influences on both static and dynamic power dissipation. Here we can observe a clear increase in static power dissipation when moving toward modern generation FPGA families. Static dissipation increases due to increase in leakage currents and because of shrink in transistor sizes. Power it is essential that the reduction of leakage effects. Concerning dynamic power consumption, the core FPGA supply voltage and node capacitance reducing with each new process node, which provides the substantial dynamic power savings over previous generation FPGAs. However, dynamic power is much greater compared to static power consumption.

Also by technology scaling, negative bias temperature instability (NBTI) is emerging as one of the other major reliability degradation mechanisms for both low and high voltage analog CMOS circuits. It occurs primarily in PMOS transistors with negative gate voltage bias and appears to be negligible for positive gate voltage PBTI in n-channel MOSFETs. NBTI occurs when PMOS transistors are negatively biased at elevated temperature, causing a shift in the threshold voltages. Over a long period, such shifts can potentially cause a significant increase in the delay of PMOS devices and results in significant degradation in the circuit speed, which leads to a potential failure. It will be found in both combinational and sequential blocks since they observe a"0" at their gates most of the time. Hence, it is important for modeling, analyzing and thus mitigating the impact of the NBTI effect on the circuit performance that determine the lifetime of CMOS devices. Due to these reasons, aging optimization is one of the other key design goal in Nano scale technology.

2. Related Work

In this section, we mainly survey the previous efforts on power reduction techniques and circuit aging optimization techniques. With the continuous trend of technology scaling, power consumption and aging has become more and more significant in the performance of today's CMOS circuits. In modern technologies, new architectural features were leading to the risk of very high power dissipation in a die. In the past many methods had been proposed for leakage power reduction like forced stack, sleepy stack, sleepy keeper, dual sleep approach etc. using techniques like transistor sizing, multi-Vth, dual-Vth, stacking transistors etc. In [**5**], these methods have been proposed for the leakage power reduction in 90nm technology. Both NBTI induced circuit degradation and standby leakage power have a strong dependency on the input patterns of circuits. In [**8**], proposed the IVC (Input Vector Control) technique, which introduced a co-simulation flow to study NBTI induced circuit degradation and leakage power, taking into account the different behaviors between circuit active and standby time.

In [**21**], proposed a fast leakage estimation technique based on biasing states for both gate leakage and sub-threshold leakage. Leakage estimation for a large circuit is complicated by the state dependence of both the gate tunneling current and sub threshold current. Power gating techniques are effective in mitigating leakage losses, which represent a significant portion of power consumption in Nano scale circuits. In [**9**], examined the variants of two representative techniques, Cut Off and Zig-Zag Cut Off and find that they offer an average of 80% and 20% in power savings, respectively, for asynchronous circuit families. In [**3**], clock-gating technique is presented for low power VLSI circuit design, which is a well-known technique to reduce clock power. By clock gating technique, clock to an idle portion is disabled, thus avoiding power dissipation due to unnecessary charging and discharging of the unused circuit. In [**22**] presented two techniques for efficient gate clustering in MTCMOS circuits by modeling the problem via Bin-Packing (BP) and Set-Partitioning (SP) techniques can achieve on average 90% savings for leakage power and 15% savings for dynamic power. NBTI in PMOS transistors has become major reliability concern in Nano meter scale design causing temporal degradation of PMOS transistors and delay of digital circuits. A novel method to characterize delay of every gate in the standard cell library as a function of signal probability of each of its input is developed. Accordingly, a technology mapping technique that incorporates the NBTI stress and recovery effects, in order to ensure optimal performance of the circuit during its entire lifetime is presented in [**16**]. In [**17**], analyzed the impact of NBTI degradation in circuit performance in terms of timing, and shows that under worst-case scenario, one can expect more than 10% degradation in the maximum circuit delay after 3 years operating time.

3. Gate Replacement Technique

Many techniques have been proposed recently to reduce the leakage power consumption. When a circuit has many logic levels, the IVC technique becomes less effective because the primary input vectors less affect the internal gates at a deep level. Hence, we prefer one of the INC techniques: gate replacement technique. This is the first research technique to achieve NBTI induced degradation mitigation and leakage power reduction simultaneously by using internal node control technique.

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Gate replacement technique replaces a gate $G(\vec{x})$ by another library gate $G(\vec{x}, sleep)$ in their Worst Leakage State(WLS), where $\vec{x}$ is the input vector at G, such that it follows:

1. $G(\vec{x}, 0) = G(\vec{x})$ when the circuit is active (SLEEP = 0);
2. $G(\vec{x}, 1)$ has smaller leakage than $G(\vec{x})$ when the circuit is in standby (SLEEP = 1).

The first condition guarantees the correct functionality of the circuit at active mode. The second condition reduces the leakage on gate G at the standby mode, but it may change the output of this gate. In the standby mode, ,it will not necessarily maintaining the circuit's functionality but at the same time, this change may affect the leakage of other gates which should be carefully considered.

Gate replacement technique belongs to the class of internal node control, but it is conceptually different from other techniques in the following aspects:

- They treat each input pin of the gates as potential places to insert multiplexers, while we consider only roots of each tree. The search space is reduced substantially.
- Their purpose of modifying a gate is to produce the low-leakage input for G's fan out gate while we aim to reduce leakage current at itself.
- They modify gates whenever necessary while we restrict this algorithm to replace gates only by the available gates in the library, and, hence, do not require gate structure modification.

3.1 Gate Replacement for Leakage

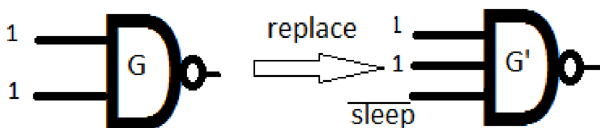

Figure 2: Gate Replacement Leakage Reduction

We call a gate at its WLS (Worst Leakage State) when its input vector leads to the largest leakage power. Regardless of the primary input vector, a large number of gates are at WLS, particularly when the circuit has high logic depth. Figure 2 shows how to replace an NAND2 gate to reduce its leakage power. The NAND2 gate is in WLS with leakage power 37.2nW, when its input is 11. We replace it with an NAND3 gate, of which the leakage power is 0.0249nW during the standby time. Then we can save up to 65.2% of the leakage power.

3.2 Gate Replacement for NBTI

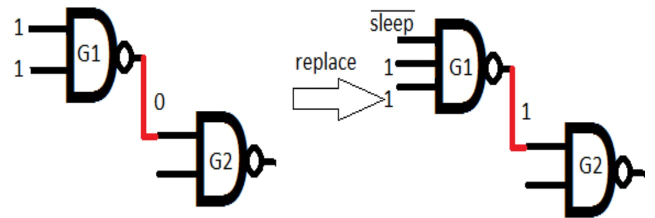

Figure 3: Gate Replacement NBTI Mitigation

The aging effect on a PMOS transistor depends on Vgs and stress time, which are both related to the input state of a gate. Experimental results show that all 1's will be the best-input pattern with the smallest NBTI induced degradation for all gate types. Figure.3 is an example that shows how to mitigate NBTI induced degradation by gate replacement. The NAND2 gate G_2's delay will be greater, when G1's output is 0 at the circuit standby time. But gate replacement technique can be applied by inserting the sleep signal. Hence we replace G_1 by NAND3 gate so that the output is changed to 1. Hence, the NBTI effect on G_2 can be optimized during the standby time.

Both the NBTI and leakage problems depends on the technology and design parameters related to the gate operations. Experimental results show that all 1's will be the best-input pattern with the smallest NBTI-induced degradation for all gate types. Similarly for reducing the leakage power, the best-input patterns for NAND/AND/INV gates are all 0's at the inputs, while for NOR/OR/BUF gates are all1's. The input pattern for minimum leakage will lead to worst NBTI- induced delay degradation; but for NOR/OR/BUF gates, the input pattern for minimum leakage will lead to best-case NBTI induced delay degradation. Therefore, we requires the control of internal node states which can be carefully chosen to meet both static power and lifetime requirements.

4. Gate Replacement Algorithm

The gate replacement algorithm is based on Direct Gate Replacement algorithm. Consider the input gates $\{G_1, G_2, \ldots. G_N\}$ which are in the topological order. SLEEP is the circuit sleep signal and $\vec{x}$ is circuit input vector and the corresponding output circuit will have same functionality when SLEEP=0 and less leakage and NBTI degradation happens when SLEEP=1.

4.1. NBTI Optimization

In the NBTI mitigation part, when we consider a gate G_i in the topological order, the G_i's critical fan-in gate G_c in the critical path is first selected. To mitigate the effect of NBTI in the critical path, the output value of G_c should be "1". If the output of G_c is "0" and there is a corresponding library gate G'_c that can replace, then we temporarily replace G_c by G'_c. After this replacement, if the output logic is changed to be "1", then we mark the replacement of G_c. Else the output is not changed to be "1", and then we will find all the fan-in

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gates of gate G_c, and try to replace them according to G_c's type, to make the output logic of G_c be "1".

4.2. Leakage Reduction

After the NBTI mitigation, all the gates are visited by a topological order again. We skip the gates that: i) are not at WLS or ii) are in critical paths and their outputs will be changed after replacement or iii) have already been visited, until we find a new gate at its WLS. Then we temporarily replace Gi and forms a new set S that includes all the unvisited gates affected by the replacement of Gi. All the newly added gates in S are temporarily replaced. The total leakage change caused by the replacement and the circuit delay at time 0 are calculated. If there is leakage reduction and the circuit delay satisfies the requirement (5% delay relaxation at time 0 caused by gate replacement is allowed), all the gates in the set S are marked as replaced and visited. Otherwise, we only mark Gi as visited. This algorithm will not finish until all the gates have been visited.

Here the optimal input vector generation phase is easily possible compared to pure IVC technique. Both NBTI mitigation part and leakage reduction part can be simultaneously performed step-by-step also further power savings also possible compared to previous techniques.

Divide & Conquer-Based Gate Replacement (DCBGR) algorithm is based on the improved gate replacement algorithm can be used for very complex circuits. First we divide the large circuit into tree circuits by deleting some connections between gates until every gate fans out to at most one gate and performing the direct gate replacement algorithm on each tree.

5. Voltage Scaling Technique

MOS transistor scaling improves its size, cost and performance. Today's fabricated integrated circuits are many times faster and occupy much less area, like today's microprocessors that contain nearly one billion transistors on a single chip. The role of supply voltage is vital for controlling the power consumption and hence reducing the power dissipation. It is reducing for each new technology generation. Scaling methods pay a significant role in reducing the power dissipation from one technology to another. There are various scaling methods used for VLSI circuits. Most common are voltage scaling, load scaling, technology scaling and transistor sizing (width scaling).

A common and very effective method of reducing the power dissipation of a circuit is to reduce its supply voltage. The dynamic power dissipation component is directly proportional to that makes this technique so effective. Power reduction is possible through the voltage scaling at a constant clock frequency. Applying a voltage scaling technique that changes the supply voltage of gates to a lower value in CMOS circuits is an effective way of reducing power consumption. Scaling down the supply voltage of a gate will cause the gate to have a longer gate delay. In order to maintain the correctness of the timing, only the gates along noncritical paths are assigned to a lower supply voltage to convert the unused slack into power savings. There is plenty of room for power reduction via the utilization of lower supply voltages on the gates of large slack. Voltage scaling algorithm for VLSI circuits utilizes the slack of each gate to scale down the voltages of the gates. It performs an iterative optimization method to scale the supply voltage of gates effectively.

6. Multi-level Voltage Scaling

The inputs of the algorithm are the circuit, which has no timing violation and a standard cell library. A set of voltage domain $V=\{V_1,V_2,\ldots Vn|Vi<Vi+1 \text{ for } i=1,2,\ldots,n-1\}$ which represents the voltages that may be applied to the gates of the circuit. Initially, the supply voltage of all gates is Vn, which is also denoted as VDDH. The lowest voltage is V_1also denoted as VDDL. The objective is to scale down the supply voltage on the gates such that the total power consumption is reduced while maintaining the same cycle time of the design.

6.1. Timing Analysis

At the beginning, we apply the timing analysis procedure to calculate the cycle time of the circuit and the slack of each gate. This cycle time is used as the timing constraint of the design in order to maintain the timing correctness of the circuit. Arrival time (A): We first calculate the arrival time of each gate. The breadth first search algorithm (BFS) is applied in a levelized manner to find the maximum delay of all paths. Each BFS starts from a PI/flip-flop and ends at a PO/flip-flop. At the starting gate of each path, the arrival time of each PI/flip-flop is the delay of the PI/flip-flop. The maximum delay among output ports of a gate is the arrival time of the gate. The maximum arrival time among all POs/flip-flops is the cycle time of the circuit.

Require time(R): Then, we calculate the require time of each gate. The BFS algorithm is applied backwards from a PO/flip-flop to a PI/flip-flop. The cycle time of the circuit is set to be the require time at each PO/flip-flop. When a gate is visited, its require time is equal to the require time of the previous gate minus the sum of the delay of the previous gate and the connected wire.

Slack(S): Finally, the slack of a gate is calculated by subtracting the arrival time from the require time of the gate. If the slack of any gate is negative then the circuit has a timing violation. In order to maintain the correctness of the timing, only the gates along noncritical paths are assigned to a lower supply voltage to convert the unused slack into power savings.

$$S=R-A$$

6.3. Power Consumption Calculation

$$P_x=\sum_{j=1}^{u}(E^i_j * f * S^i_j) + 0.5*\sum_{k=1}^{v}(C^0_k * V_x^{2} * f * S^0_k)$$

The dynamic power consumption of a gate, denoted as P_x where u and v are the numbers of input and output pins of gate x. E^i_j is the power consumption of the jth input pin. The

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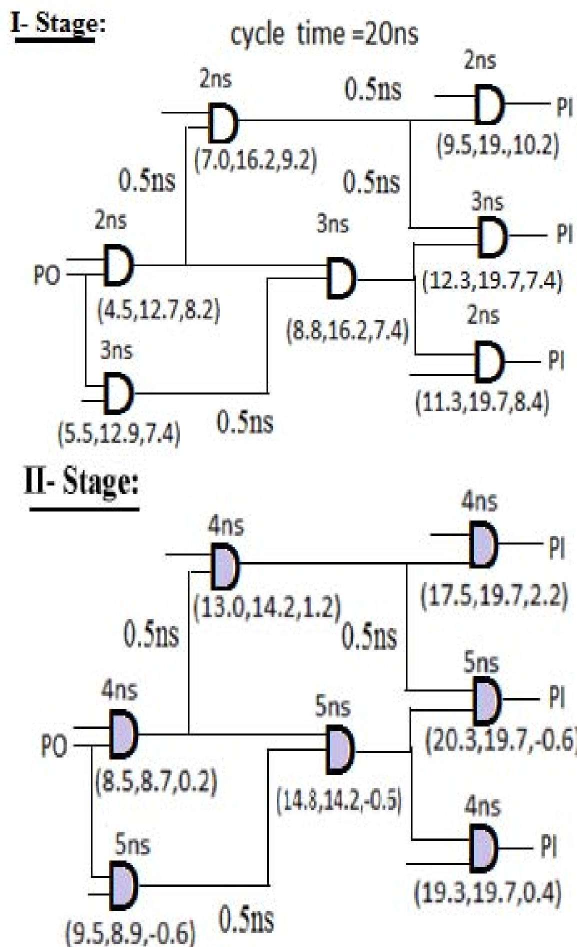
values of E^i_j may be extracted from the lookup table in the library according to the total capacitance of fan-out load. f represents the frequency of the circuit. S^i_j and S^0_k represent the switching activity of the jth input pin and the kth output pin, respectively.C^0_k is the loading capacitance on the kth output pin. The value of C^0_k is the sum of the capacitances of the fan-out net and the driven pins of the net. The capacitance of each net is estimated by applying wire load model. V_x represents the supply voltage at gate x. For example, if x is a VDDH/VDDL gate then V_x equals to VDDH/VDDL. The total power consumption of the circuit is calculated by the sum of power consumptions all individual gates.

We assume that the input circuit has no timing violation. This algorithm will reduce the power consumption of the circuit by scaling down the supply voltages of gates while maintaining the timing correctness of the circuit. Here we apply a greedy approach that scales down the supply voltages of as many gates as possible. The VDDL gates will be fixed at the lowest voltage and the rest of gates are referred to "scalable gates."



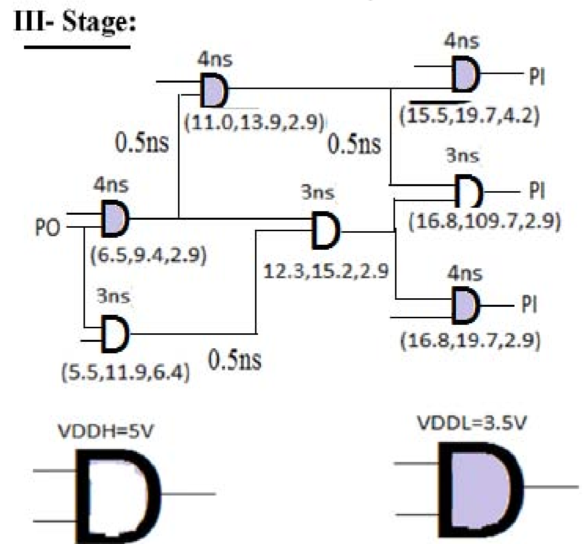


Figure 4: Example of multilevel voltage scaling technique

First, we scale all gates in the net list to the lowest voltage as shown in figure-4. An LC is needed between a VDDL and a VDDH gate to prevent the creation of a static current. LCs are inserted before the primary output gates. Static timing analysis is performed to calculate the slack of all gates. The supply voltages of all gates with negative slacks are scaled up to the next higher supply voltage. The net list is adjusted by inserting or removing LCs according to the vicinity connectivity of the voltage scaled gates. Then, we perform timing analysis again to recalculate the slack of each gate. The delays of LCs and nets along the path are also included in the timing calculation. Then the slacks of these gates are updated. If any gate with negative slack is found, then the supply voltage of the gate is scaled up to the next supply voltage. This process is repeated until the slacks of all gates are positive or zero.

7. Implementation of Proposed Method

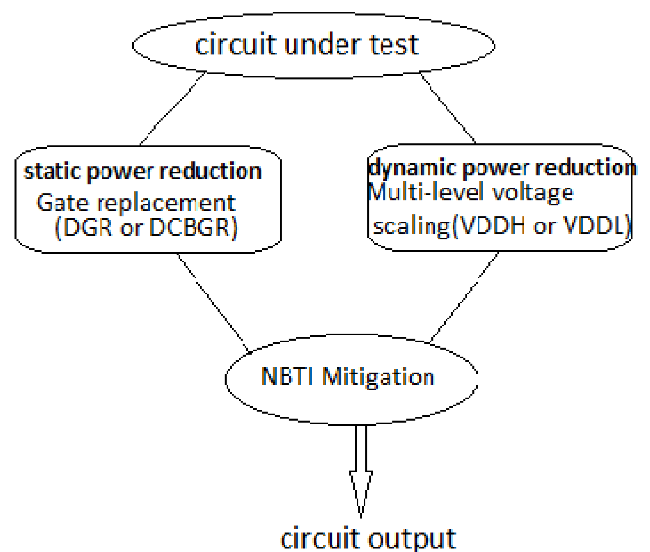


Figure 5: Block Diagram of the proposed method

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The block diagram of proposed method is shown in figure-5. The major power in CMOS circuits is consumed during switching which is termed as dynamic power dissipation. This absorbs more than 60% of the overall power in the circuit. However as the technology scales down, sub threshold leakage have very much influences on dynamic power dissipation due to the reduction in threshold voltage and device geometry. During switching VDD supplies the circuit's parasitic capacitance which results most of the power is consumed as dynamic power. So this voltage should be controlled within tolerable levels. The static power dissipation occurs when the inputs applied to a logic gate and the corresponding output will not changing. Current researches shows that the static power dissipation becomes comparable to the dynamic power dissipation as the supply voltage and technology scales down. In this work, a new technique is proposed that combines Voltage Scaling and Gate Replacement technique to suppress both dynamic and static power dissipation and hence reducing the overall power consumption. The Voltage Scaling technique reduces dynamic power dissipation without degrading the circuit performance while leakage or static power dissipation is lowered with gate replacement technique. In addition, aging optimization is achieved by gate replacement technique which improves reliability as well as performance.

8. Analysis and Results

The Gate Replacement technique is implemented on ISCAS 85: C-17 benchmark circuit and simulated using ModelsimSE 6.3f and leakage reduction and aging optimization results were observed and verified. Tanner13 Tool is used for obtaining the leakages values for 2 input nand gate and 3 input nand gate.

8.1. Analysis of Gate Replacement Technique

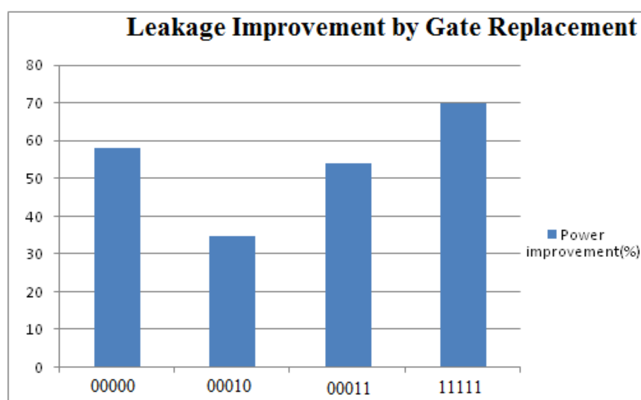

Figure 6: Leakage Comparison on Different Inputs

From the design view, the gate replacement technique does not require gate structure modification and is compatible with the current standard cell based design flow. This technique can also be combined with optimal input vectors at the primary inputs for leakage power minimization and NBTI optimization. The gate replacement technique introduces delay, power and area overhead which can be controlled by adding delay and area constraints in the optimization algorithms, or by performing transistor resizing. The delay constraint is set to be less than 5% of the original delay increase at time 0 after applying this technique. The sleep signal generation and distribution is a general problem for all the circuits which are performed in logic level. Such issues should be carefully handled at the physical design stage, together with other existing standby time leakage reduction techniques. Gate replacement and other INC techniques are effective for gates in standby mode which cannot be effective in active mode. When the circuit is active, they do not change any gate outputs and the circuit maintains the original functionality. Thus INC techniques provides no benefit in active time.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		138
Vccint 5.00V:	26	132
Vcco33 3.30V:	2	7
Clocks:	9	45
Inputs:	2	12
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 5.00V:	15	75
Quiescent Vcco33 3.30V:	2	7

Figure 7: Dynamic power results of Gate Replacement

8.3. Analysis of Voltage Scaling Technique

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		87
Vccint 3.50V:	23	80
Vcco33 3.30V:	2	7
Clocks:	6	22
Inputs:	2	6
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 3.50V:	15	53
Quiescent Vcco33 3.30V:	2	7

Figure 8: Dynamic power results of voltage scaling

The above figure shows the dynamic power comparison results for circuit after gate replacement and voltage scaling. In gate replacement technique, there is not much dynamic power overhead because the sleep signal remains constant at active mode and will not cause any additional switching

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activities. From these figures, dynamic improvement by voltage scaling is clearly observed.

In the proposed voltage scaling technique, we use dual voltage domains use 5V and 3.5V respectively. Here many gates are assigned to VDDL gates and the number of VDDH gates is reduced. After performing this technique, on average, the problem size is reduced compared to the original size. The amount of reduction depends on the timing tightness of the paths in the circuit. More paths with looser timing will exhibit a greater reduction in the problem size. On average, 63.04% of the total power of the original circuit is saved. This algorithm successively scales gates from high voltage to low voltage such that the slacks of gates are decreased. It shows that this algorithm utilizes the slack of each gate to scale down the voltage of the gates. Even though the voltages of all gates along these paths have been scaled to the low supply voltage, the slacks of these gates are still much larger than the slacks of other gates. This implies that the supply voltages of these gates could be scaled further downward. Using more voltage domains saves more power, it needs more voltage islands and the designer must make extra efforts to accommodate the extra voltage islands. Therefore, for the proposed algorithm, if the most comfortable supply voltage for each case is known, the use of dual supply voltages is a good choice for considering both power and effort saving.

9. Conclusion

The proposed work can be applied not only to the combinational circuits but also for more complex sequential circuits they can be applied in every application from gate level to processor level. Power reduction and NBTI mitigation can also be improved by combining the advantages of multilevel voltage scaling as well as gate replacement algorithms. Initially static leakage improvement is performed by inserting sleep signal on the corresponding logic gate inputs and further dynamic power improvement can be accomplished by applying high level and low level supply voltages for the required gates. If any delay occurs in any portion of the circuit then gate replacement technique is applied for NBTI optimization. Thus maximum leakage reduction and delay improvement can be achieved by voltage scaling and gate replacement techniques. The circuit was analyzed and simulated using Modelsim and Xilinx ISE 8.1 to estimate the switching power and leakage power, thus overall power consumption were observed and verified.

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