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A Modified NoC Router Architecture with Fixed Priority Arbiter

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Abstract: ***NoC is an approach in designing communication subsystems between intelligent property (IP) cores in SOC with greater efficiency. RKT router switch that handles accurate localizations of the faulty parts of the dynamic NoCs. The RKT-NoC switch is highly reliable when compared with ordinary NoC due to the addition of error detection mechanism in the design and it avoids the deadlock and livelock problems.NOC means network on chip is a new method for on chip communication to solve a problem that challenges system on chip. The proposed method adoptes an fixed priority arbiter. Arbiter is used in network on chip when number of input are requested for same output port, the arbiter has generate the grant signal on the basis of that number of input port getting a priority and the input port transmit a packet to output port. The proposed methods distinguish the path of data packets thereby avoiding the collision between the data packets. The arbitration should guaranteed the fairness in scheduling, avoid starvation, and provide high throughput.***

Keywords: Deterministic algorithm, Fixed priority arbiter, Network on chip.

1. Introduction

As the area and speed on a single chip now faces the big challenge on a single chip, more and more processing elements now are placed on System on chip. Network-on-chip (NoC) is a new method for on chip communication to solve the problem that challenges the system on chip. Network on chip (NoC) is a communication subsystem on an integrated circuit between intellectual property (IP) cores in an system on chips (SoC) .NoC is an emerging paradigm within a large VlSI systems. NoC has advantages on architecture, performance, -on-chip (NoC), reliability. NoC are designed using networking theory and methods to on-chip communication, which brings considerable improvements over conventional bus architecture and crossbar interconnections. To increase system scalability and the power efficiency of complex SoCs compared to other designs the NoC can play the major role. Network-on-Chip (NoC) is an upcoming and challenging field of technology for implementing on VLSI and the ULSI platform on single silicon chip. In this concept many modules such as processor cores, memories, multiplexers and specialized IP blocks exchange data using a network as a transportation subsystem for the information [1]. A NoC is designed from multiple point-to-point links interconnected by switches (routers), such that messages can be relayed from any source module to any destination module over several links, by making routing decisions at the switches. A NoC is analogous to a modern telecommunications network, using digitized switching over multiplexed links for efficient communication over the internal links. The NoC medium features a high level of modularity, flexibility, and throughput.But the NoC is viewed as the ultimate solution to avoid problems that will arise because of the growing size of the chip.

A generic NoC architecture is characterized by the number of routers, each of which is attached to processing elements in the array, the bandwidth of the communication channels between the routers, the topology of the network and the mechanism used for packet forwarding. The topology of the network is defined through the arrangement of routers and processor on the device and the way those processors are connected together. One of the most used topology is the 2-D mesh network, because it naturally fits the tile-based architecture on the chip, and the main components which used to build this Network on Chip is router and processing element. It uses the wrapper to communicating between them and the router uses buffer, control logic and output arbiter to make the proper routing function. The physical interconnection on a chip becomes a primary factor which limits the performance and power consumption. As the switch speed of crossbar switch increases rapidly, on big problem we should resolve is to implement a fast and fairness arbiter to maximize the switch throughput and timing performance for Network on chips. Arbiter is used in network on chip when number of input are requested for same output port, the arbiter has generate the grant signal on the basis of that number of input port getting a priority and the input port transmit a packet to output port. In this paper we have design round robin arbiter for NOC architecture. The proposed arbiter detects buffer status of input ports and changes priorities of the input port dynamically to enhance the performance of the router [2].

2. Previous Works

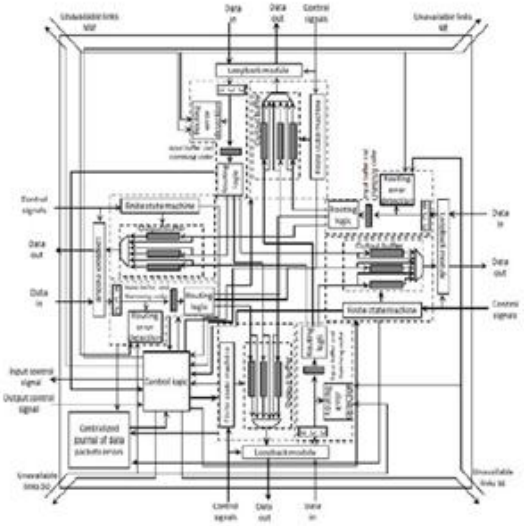

Figure 1: RKT Switch

The previous work is a new reliable NoC-based communication approach called RKT-NoC. The RKT-NoC is a packet switched network based on intelligent independent reliable routers called RKT-switches. The architecture of the RKT switch is depicted in Fig. 1. The RKT-switch is characterized by its architecture having four directions (North, South, East, West) suitable for a 2-D mesh NoC. The PEs and IPs can be connected directly to any side of a router. Therefore, there is no specific connection port for a PE or IP. The proposed detection mechanisms can also be applied to NoCs using five port routers with a local port dedicated to an IP. However, the major drawback of these architectures is when the local port has a permanent error and the IP connected to it is lost or needs to be dynamically moved in the chip because of the dynamic partial reconfiguration. On the contrary, for the four-port RKTNoC, an IP can replace several routers by having several input ports and hence be strongly connected in the network [3].Moreover, by using dynamic partial reconfiguration and IPs strongly connected in the NoC, no one fault location is more catastrophic than another.

A.Routing Logic

Routing is the important point to be considered, which shall act as the backbone to avoid deadlock and live lock. The routers are address in the matrix format .There were two types of logic used namely Deterministic and the adaptive or both the types can be combined to be used for dynamic reconfigurable network structure. A deterministic routing algorithm provides a unique path from a source to destination. XY-routing also called dimension ordering routing is a simple deterministic routing algorithm, where messages are transmitted fully in each dimension, beginning with the lowest dimension available. In a 2-D mesh network, XY-routing first routes packets along the X-axis. Once it reaches the destination's column, the packet is then routed along the Y-axis until the destination's line. Therefore, any packet moving in the Y direction can never return to the X-direction. This routing logic will follow a loopback module to avoid deadlock and livelocks.

B. Loopback Module

The RKT switch consists of a loopback module block which is used to make a new path for the packets by looping back through another port. It is done if and only if the current router found any fault in the neighbour router to which the packet has to be sent.

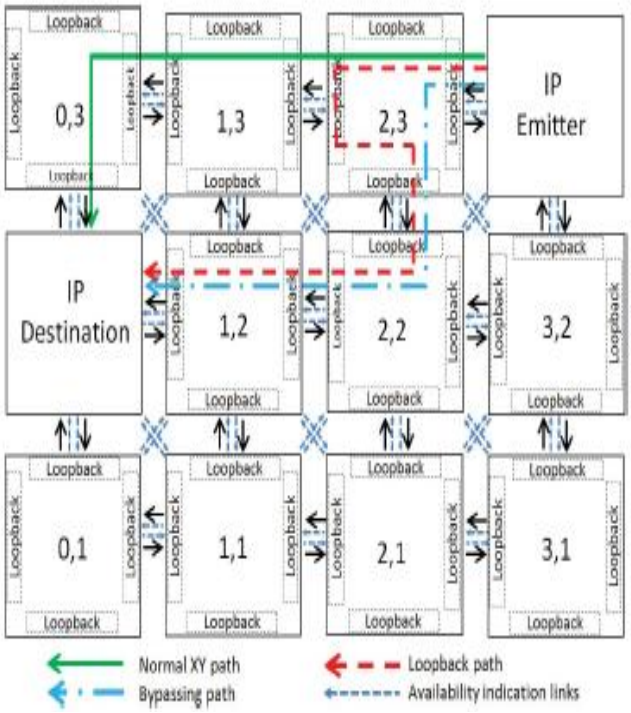

Figure 2: Loop backing of data packets

C. Routing Error Detection

The occurrence of error is not only due to the change in the value of the message being sent it also occur due to the wrong routing path, due to the wrong routing path the live lock and deadlock occurs. Hence to avoid this particular routing error detection is added with the RKT-noc When a message is passed from one IP core to another IP core via certain router it has to check whether it is operating correctly for that purpose a router has to check initially that the router is the current operator and whether the previous router obeys the XY algorithm, if it obeys the algorithm then the router conformed that the router has no error or else further it checks the availability of the router in the path by checking the diagonal availability indication. On checking that availability link if the router in the path is unavailable then checks weather the input for this router is for bypass operation if not it says the router has an error or else it confirmed that the router has no error.

3. Proposed Design

The NoC's switches should provide high speed and cost-effective contention resolution scheme when multiple packets from different input ports compete for the same output port. A fast arbiter is one of the most dominant factors for high performance NoC switches [4].The proposed technique adoptes an arbiter. For the above reasons the analysis of the performance of the arbiters are significantly meaningfulness in the design of Network-on-chips.

A. Arbiter

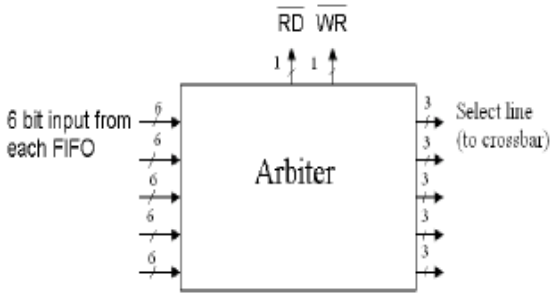

Figure 3: Basic Structure of Arbiter

Arbiter is used in network on chip when number of input are requested for same output port, the arbiter has generate the grant signal on the basis of that number of input port getting a priority and the input port transmit a packet to output port. The arbiter trap the source and destination address from the output of buffer and generate the control signal so that input data from source side sending to the output port. Arbiter controls the arbitration of the ports and resolve contention problem. It keeps the updated status of all the ports and knows which ports are free and which ports are communicating with each other. Packets with the same priority and destined for the same output port are scheduled with a fixed priority arbiter. The arbiter will release the output port which is connected to the crossbar once the last packet has finished transmission. So that other waiting packets could use the output by the arbitration of arbiter. In proposed work, fixed priority arbitration algorithm use to assign priorities when many input ports request the same output. Output signal generated by arbiter is read, external clock, three bit select lines for crossbar switch to select output channel. External clock signals which is indication for next connecting router that data is now available on output port of source router[3]. When it is high, it means data is now available on output port of that router. Read signal generated by considering current status of signal of that port only. Read signal is high only when FiFo empty. Signal is low it means buffer is not empty, some data is store in Arbiter generates three bit select lines to select output channel for outputting data out of router. Steps follow to generate three bit select lines to properly route in coming packet out of router given as below. First compare three bit destination address to select output channel for dataflow out of router. Next three bit are source address indicate the input channel from where packet is transmitted.

B. Fixed Priority Arbitration

Fixed priority arbiter always authorizes the requiring input port with the highest priority when requiring contention happens. The input ports with lower priority may rarely be authorized which results in extremely unfair. Supposing in a given period of time, there was many input ports request the same output or resource, the arbiter is in charge of processing the priorities among many different request inputs. The arbiter will release the output port which is connected to the crossbar once the last packet has finished transmission. So that the other waiting packets could use the output by the arbitration of arbiter. Depending upon the control logic arbiter generates select lines for multiplexer based crossbar and read or write signal for FIFO buffers. The Fixed priority arbiter is a common arbitration scheme. Each requester is assigned a fixed priority, and grant is given to the active requester with he highest priority. Fixed Priority arbiters are very common when choosing between just a few requesters. For example a maintenance port may always be lower priority than the functional port.ECC corrections may always be higher priority than all other requests.

C. NoC Router with Arbiter

Network-on-chip (NoC) is considered as a promising paradigm to overcome the communication bottleneck of future multicore systems. As a basic component in on-chip router, arbiter has a big impact on the performance of router. A NoC comprises routers and interconnections allowing communication between the Pes and IPs. The NoC relies on data Packet exchange. A NoC is a communication subsystem on integrated on chip. The physical interconnection on a chip becomes a primary factor which limits the performance and power consumption. As the switch speed of crossbar switch increases rapidly, on big problem we should resolve is to implement a fast and fairness arbiter to maximize the switch throughput and timing performance for network on chips[4],[5].The heart of an on-chip network is the router, which undertakes crucial task of coordinating the data flow. The router operation revolves around two fundamental regimes: (a) the data path and (b) the associated control logic.

The data path consists of number of input and output channels to facilitated packet switching and traversal. Generally 5 input X 5 output routers is used. Out of five ports four ports are in cardinal direction (North, South, East, West) and one port is attached to its local processing element. Like in any other network, router is the most important component for the design of communication back-bone of a NoC system. In a packet switched network, the functionality of the router is to forward an incoming packet to the destination resource if it is directly connected to it, or to forward the packet to another router connected to it. It is very important that design of a NoC router should be as simple as possible because implementation cost increases with an increase in the design complexity of a router. The design of router mainly consists of three parts:

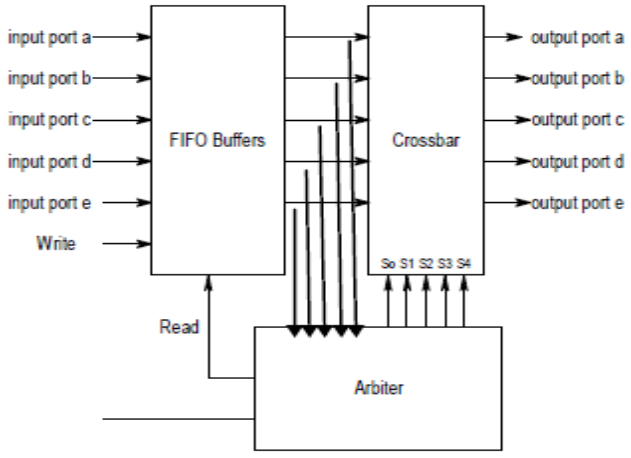

Figure 4: Block Diagram of NoC Router with Arbitraion

1. FIFO
2. Arbiter
3. Crossbar

Many researchers focused on developing various arbitration schemes in order to achieve an efficient allocation and reduce packet latency. A lot of arbiters have been proposed in the routers of computer network such as round robin arbiter, fixed priority arbiter, lottery arbiter, token ring arbiter and so on. Round robin arbiter treats each input port fairly and guarantees fairness in scheduling. Using round robin arbiter, each input port have an equal chance to own the output port and the starvation problem can be solved. However, round robin arbiter is too fair and may cause low efficiency for some input ports. Fixed priority arbiter always authorizes the requiring input port with the highest priority when requiring contention happens. The input ports with lower priority may rarely be authorized which results in extremely unfair. Lottery arbiter offers input ports certain numbers of lottery as their priority level. Input port with more lotteries has bigger probability to win the output port. However, if the number of lotteries is static, some input ports which have little lotteries may be hardly responded under heavy traffic load. Token ring arbiter cannot guarantee correctness and may miss some requests from the different input buffers[6],[7][8].

Arbiter is one of the key components in the on-chip router. It can determine the output sequence when output contention happens. If packets arrive at different input ports but need to be dispatched into the same output port simultaneously, a output contention will happen. In order to solve the contention, an arbitration mechanism is necessary to allow only one input port to access the output port. Most arbiters are unconcerned with buffer status and authorize the input port by a determinate mechanism. These arbiters may cause head-of-line blocking problems if the input port with full buffer cannot be authorized preferentially. Arbiter controls the arbitration of the ports and resolve contention problem. It keeps the updated status of all the ports and knows which ports are free and which ports are communicating with each other. Packets with the same priority and destined for the same output port are scheduled with a Fixed priority arbiter. The arbiter will release the output port which is connected to the crossbar once the last packet has finished transmission. So that other waiting packets could use the output by the arbitration of arbiter.

2D mesh is the most popular topology for Network-on-Chip which has good scalability. The communication data named packet can be transferred by the on-chip routers and links in 2D mesh NoC. On-chip router is the core component in the NoC and has big impact on system performance Fig. l shows a typical 2D mesh NoC and the corresponding router architecture. Wormhole router is the one of the most commonly used on-chip routers in NoC. It is easy for implementing and suitable for on-chip network. A typical wormhole on-chip router with dedicated buffer per input port is shown in fig.5.

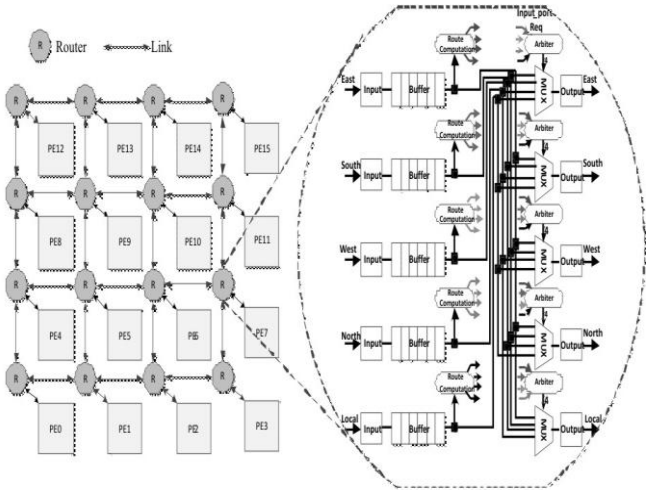

Figure 5: Cross Section of NoC Router with Arbiter

In the wormhole router, each packet is divided into small unit called flit. Head flit proceeds through all the stages while body and tail flits skip route computation and output arbitration stages[9],[10]. Body and tail flits inherit the output port allocated to the head flit. The last flit in a packet, called tail flit, releases the reserved output port that have been reserved by the header flit of that packet, when it departs the current router. The route computation determines deliver direction of the packet according to the destination of the head flit and the routing algorithm. Route computation sends request to the arbiter after determining deliver direction. Arbiter grants the request and connects output port with input port by MUX.

4. Synthesis Results and Performance Analysis

A. Synthesis Results

The results presented are obtained considering with and without arbitration of data packets. In the figure 5 the input port source addresses requested for different output port destination address so there is no contention in this case there is no role of arbiter the inputs are getting the control signal so that they transmit the packet to the destination. In the figure 6 fixed Arbiter Assign the Priority. On the basis of that if the east port has highest priority and west port has lowest priority, then firstly east port transmit the data so arbiter generate the control signal & packet transmitted from source to destination. Same way for all port. Below

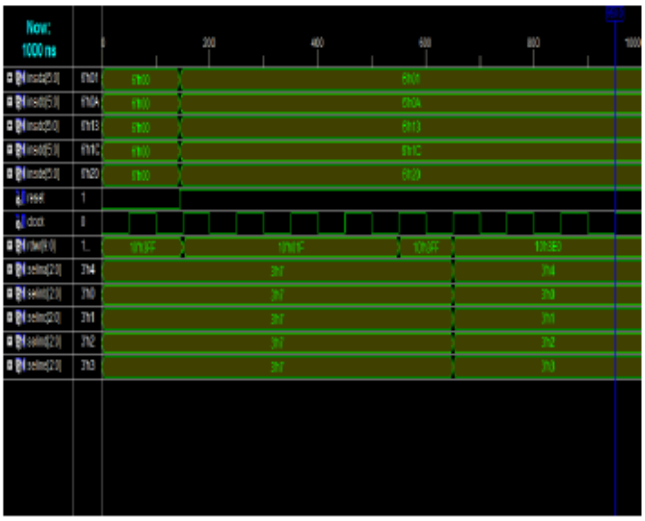

Figure 6: Without Contenion Waveform

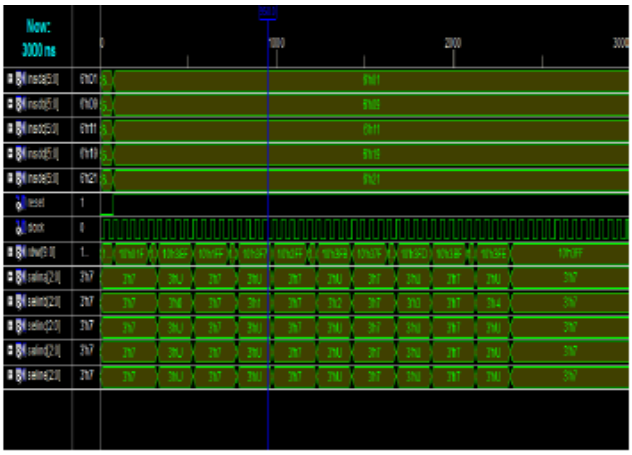

Figure 7: Contention Waveform

waveform shows the simulation result of all input port request for same output port. In this paper after synthesize we found the area gate count is 33,489 and power consumption is 7mW.

B. Performance Evaluation

1) Throughput

The maximum throughput of an RKTNoC depends on the data bus width of *n* bits, the working frequency *f*, the number of IP NIP, and the FIR. The Throughputmax is given by 3 in the case of NIP being connected by assuming they are connected to the NoC boundary.

$$\text{Throughput}_{max} = N_{IP} * n * \text{FIR}_{max} * f \quad (3)$$

By considering one RKT-switch with a data bus size of 64 and 4 IPs connected, and a maximum operating frequency for the Virtex VII FPGA technology, the Throughputmax is 41.72 Gbit/s. Figure 8 shows the throughputmax of a single RKT switch connected to four IPs for different data bus widths and operating frequencies. Figure 9 shows the Throughputmax of several RKT-NoCs connected to the maximum number of IPs and for different data widths. For instance, the 4 × 4 RKT-NoCis surrounded by 16 IPs. These

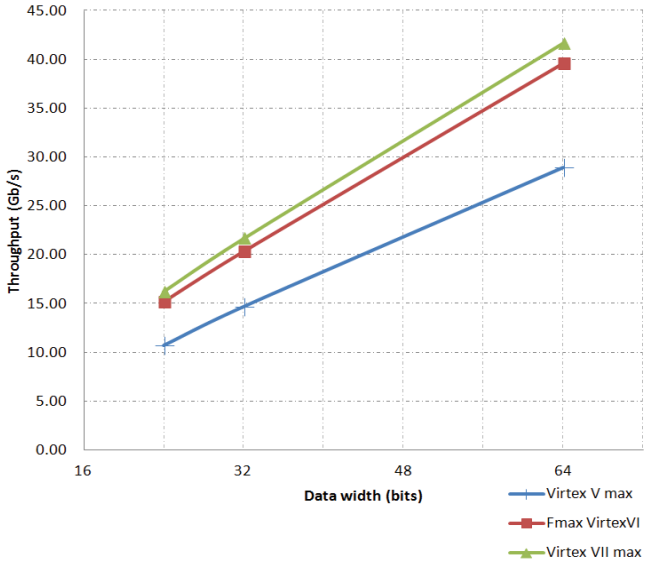

Figure 8: Throughput of one RKT-switch for different data widths

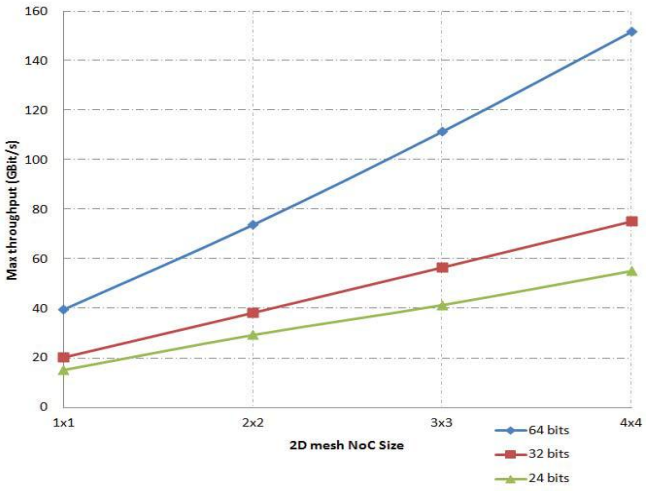

Figure 9: Maximum throughput of the RKT-NoC for different 2-D mesh sizes and data widths.

throughputmax results are given considering the maximum working frequency of the synthesis results of considering the Virtex VI technology. It can be noticed that for a 3 × 3 RKT-NoC using 64 b, the Throughputmax is 111.5 Gbit/s.

5. Conclusion

An improved NoC architecture with fixed priority arbiter is proposed in this paper. NoC means Network on Chip is a new method for communication to solve a problem that challenges system on chip. In router, Arbiter is used in network on chip when number of input are requested for same output port, the arbiter has generate the grant signal on the basis of that number of input port getting a priority and the input port transmit a packet to output port. Hence our proposed arbiter is suitable for NoC design which needs high speed cross bar switches and router in them.

6. Acknowledgment

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