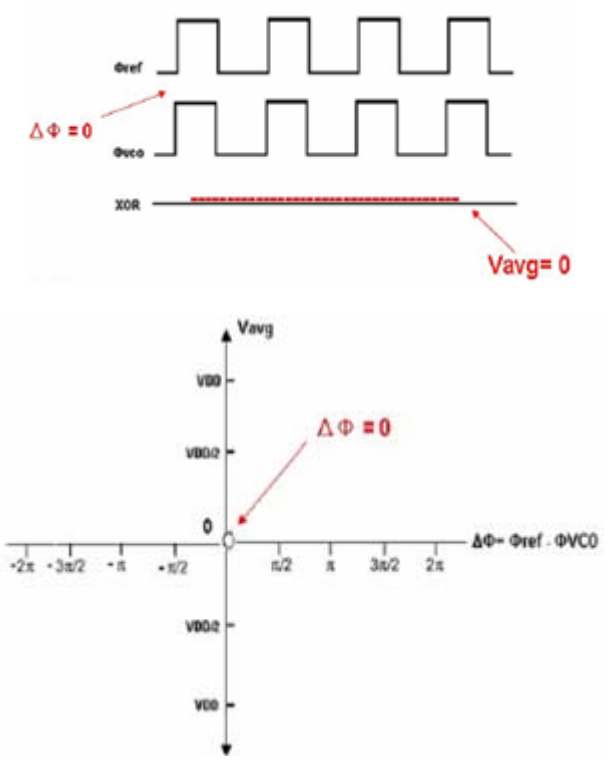


Figure 4.2

The average output, Vavg, from the XOR gate is zero for this case. The XOR input/output characteristic graph is a plot of Vavg versus the phase difference. Figures 2.1(c) and (d) plot the accumulation of points from the phase differences zero, Π/2, and Π. The final graph is shown below. This is the XOR PD characteristic plot. This plot enables us to observe the PD output for a range of phase differences.

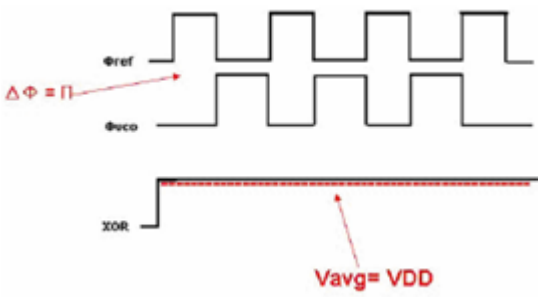
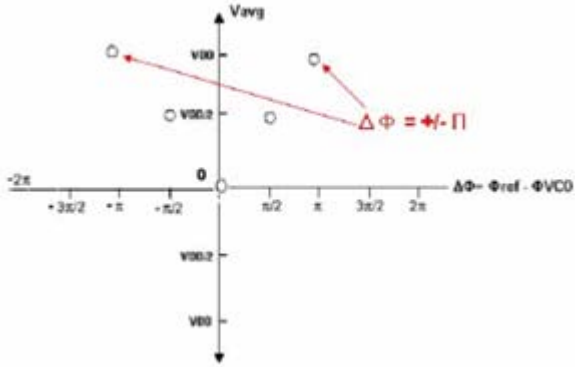


Figure 4.3: Phase Difference = Π/2



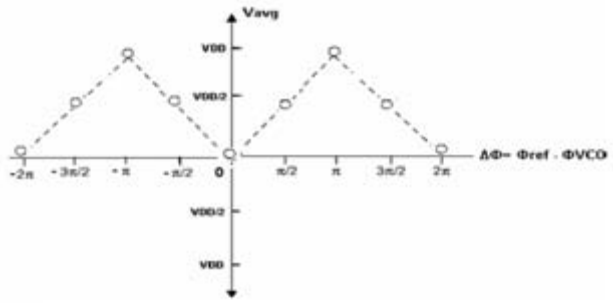


Figure 4.4: Characteristic Graph of phase differences ranging from 0 to 2Π

The XOR PD as shown above in Figure 4.1 –4.4 is a very simple implementation of a PD, however; its major disadvantage is that it can lock onto harmonics of the reference signal and most importantly it cannot detect a difference in frequency.To take care of these disadvantages, we implemented the Phase Frequency Detector,which can detect a difference in phase and frequency between the reference and feedback signals. Also, unlike the XOR gate PD, it responds to only rising edges of the two inputs and it is free from false locking to harmonics. Furthermore, the PFD outputs either an “up” or a “down” to the CP.

4.1 PFD Block Diagram

The block diagram and circuit schematic are shown below in Figures 4.5 and 4.6 respectively.

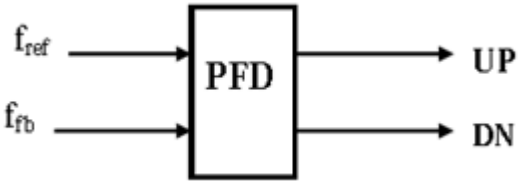


Figure 4.5: Phase Frequency Detector Block Diagram

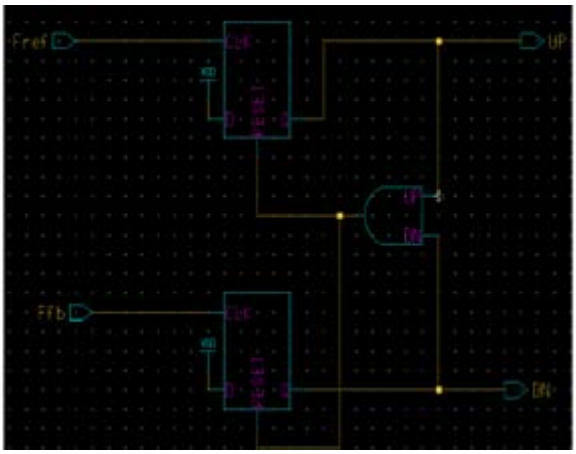


Figure 4.6: PFD Circuit

The PFD design uses two flip flops with reset features as shown in Figure 4.6. The inputs to the two clocks are the reference and feedback signals (fref and ffb). The D inputs are connected to VDD—always remaining high. The outputs are either “UP” or “DN” pulses. These outputs are both connected to an AND gate to the reset of the D-FF’s. When both UP and DN are high, the output through the AND gate is high, which resets the flip flops. Thus, both signals cannot

be high at the same time. This means that the output of the PFD is either an up or down pulse—but not both. The difference in phase is measured by whichever rising edge occurs first.The PFD circuit above in Figure 4.6 can be analyzed in two different ways—one way in which fref leads ffb and the other in which ffb leads fref. The term "lead" in this case means that the signal is faster or in the lead of the other. The first scenario mentioned above is when the reference leads the feedback signal as shown in Figure 4.7

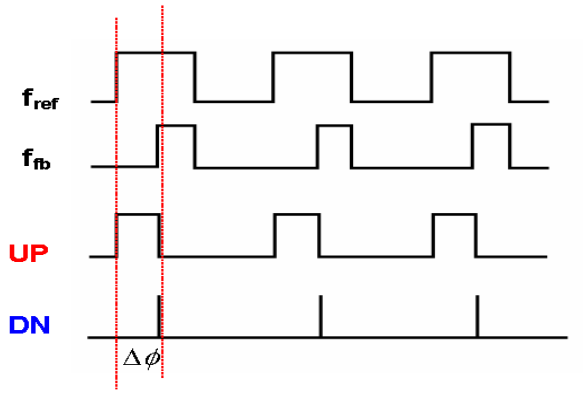


Figure 4.7: fref leads ffb

When fref leads ffb, an UP pulse is generated. The UP pulse is the difference between the phases of the two clock signals. This UP pulse indicates to the rest of the circuit that the feedback signal needs to speed up or "catch up" with the reference signal. Ideally, the two signals should be at the same speed or phase. The other scenario is when feedback signals leads the reference signal as shown in Figure 4.8

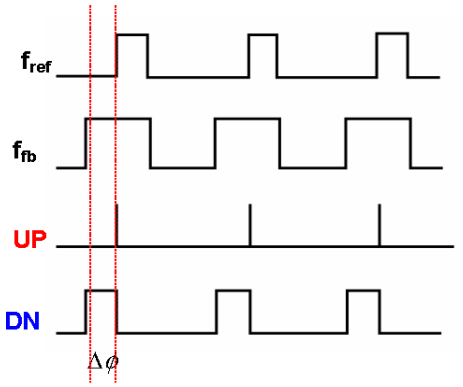


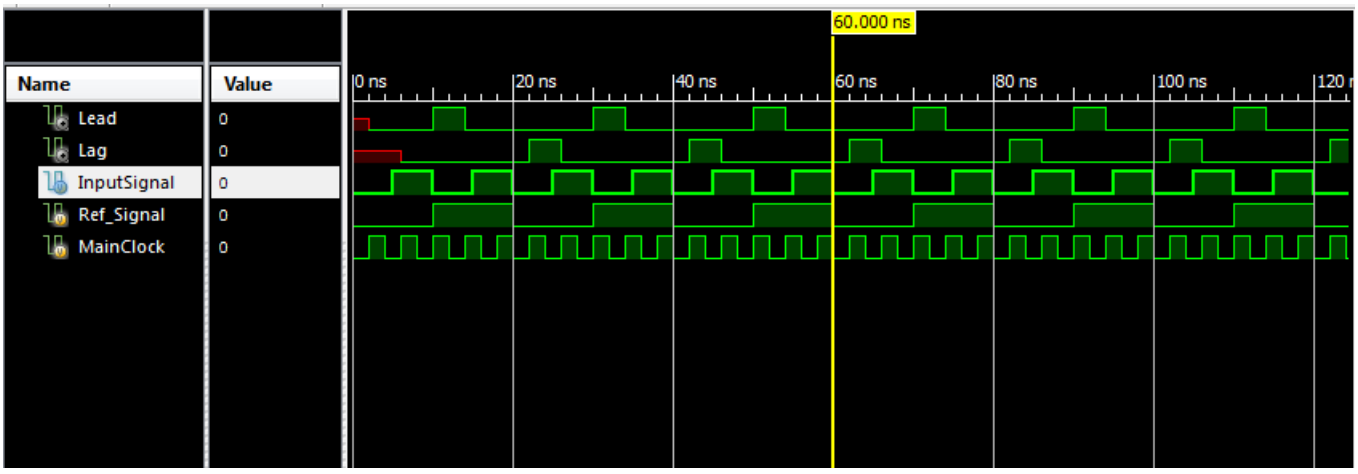
Figure 4.8: fref lags ffb

When the feedback signal leads the reference signal, which generates a DN signal. This DN signal indicates to the rest of the circuit that the feedback signal is faster than the reference signal and needs to slow down.In the actual design, the UP and DN signals were not as discrete as the ones shown above in Figure 4.7 and 4.8. Since the transistor sizes in the DFF and the AND gate were so small(size ratio of W/L = 3.4µ/1.6µ) and because the transistors were used in digital circuitry, the transistors could not switch fast enough at the frequency we were using (~100's MHz). Thus, two inverters were placed at the outputs of the UP and DN signals, in order to make the signals go to discrete low and high levels (0-VDD).

5. Simulation Results

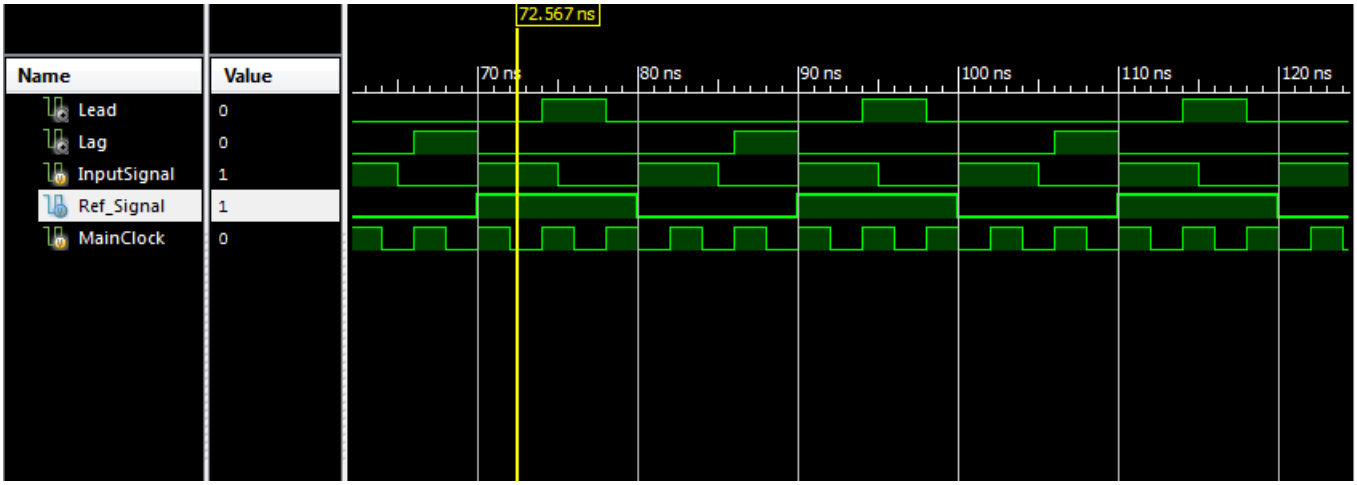
5.1. Example 1

If Ref signal = 0
Input signal = 0
Main clock=0



5.2. Example 2

If Ref signal = 1
Input signal = 2
Main clock=0



6. Advantages & Disadvantages

6.1 Advantages

The PFD is an improvement over the phase comparators of early PLLs in that it also provides a frequency error output as well as a phase error.

6.2 Disadvantages

6.2.a)Dead Zone

Dead-zone is due to small phase error. When the phase difference between PFD's input signals, the output signals of the PFD will not be proportional to this error. The reason of this problem is the delay time of the internal components of the flip-flop and the reset time that need s the AND gate to reset both flipflops. Figure 6.1 illustrates the dead zone problem. When the two clocks are very close to each other (small phase error), due to the delay time the reset delay, the output signals UP and DOWN will not be able to charge and no output will signal leading to losing this small difference.

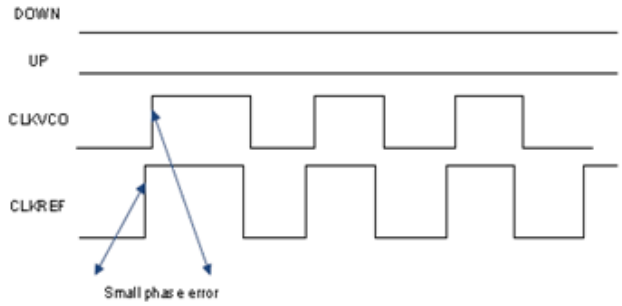


Figure 6.1: Dead Zone

Plenty of solution has been done for this problem some of them reduce the delay time in the internal components of the PFDs, other solution eliminate the reset path by implementing new reset techniques that will not create a delay and produce a high speed PFDs

7. Applications

1. The MCH/K12140 is a phase frequency−detector intended for phase−locked loop applications which require a minimum amount of phase and frequency difference at lock.
2. The MC12040 is a logic network designed for use as phase comparator for MECL-compatible input signals.
3. Phase Frequency Detectors for Fast Frequency Acquisition in Zero-dead-zone CPPLLs for Mobile Communication Systems
4. Frequency Multiplications

8. Conclusions

A phase-frequency detector is an asynchronous sequential logic circuit originally made of four flip-flops. PFD(Phase Frequency Detector) is a circuit that measures the phase and frequency difference between two signals, i.e. the signal that comes from the VCO and the reference signal. If there is a phase difference between the two signals, it generates "up" or "down" synchronized signals to the charge pump/ low pass filter. The PFD is an improvement over the phase comparators of early PLLs in that it also provides a frequency error output as well as a phase error. The problem of Dead zone can be eliminated by reduce the delay time in the internal components of the PFDs& by eliminating the reset path by implementing new reset techniques that will not create a delay and produce a high speed PFDs. The main applications of PFDs are that they are used in Mobile Communication Systems, motor control, radar & telecommunication systems, servo mechanisms, and demodulators In this project the use of a Phase Frequency detector in PLL application is explained. This paper demonstrates techniques for designing PFDs .The output waveforms were executed using the Xilinx software.

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