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# High Speed Convolution and Deconvolution Algorithm based on Ancient Indian Vedic Mathematics

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**Abstract:** ***In Digital Signal Processing, the convolution and deconvolution with a very long sequence is ubiquitous in many application areas. Both operation consume much of time.So our focus to develope more advance and simpler techniques. This paper presents a direct method of computing the discrete linear convolution, circular convolution and deconvolution.The most significant aspect of the proposed method is the development of a multiplier and divider architecture based on Ancient Indian Vedic Mathematics sutras Urdhvatriyagbhyam and Nikhilam algorithm. The implementation of linear convolution and circular convolution using vedic mathematics is functionally verified using Modelsim software and analyze on Altera FPGA platform using Quartus 2 software, parameter like area, speed and power will be compared to their implementation using conventional multiplier & divider architectures.***

**Keywords:** Convolution, Deconvolution, Vedic Mathematics, VHDL

## 1. Introduction

Convolution and deconvolution is frequently used operation in DSP .However, beginners often struggle with convolution and decovolution because the concept and computation requires a number of steps that are tedious and slow to perform. For engineers ,complexity and excess time consumption are always the major concern which motivates us to focus on more advance and simpler techniques .Therefore many of researchers have been trying to improve performance parameters of convolution and deconvolution system using new algorithms and hardware. .

Vedic Mathematics provides unique solution for this problem. Many engineering application areas use this Vedic Mathematics, especially in signal processing. It has 16 sutras and sub-sutras which cover all the branches of mathematics such as arithmetic, algebra, geometry, trigonometry, statistics etc. Implementation of these algorithms in processors has found out to be advantageous in terms of reduction in power and area along with considerable increase in speed requirements.These Sutras are given in Vedas centuries ago. To be specific, these sutras are described in ATHARVA-VEDA. The sutras and sub-sutras were reintroduced to the world by Swami Bharati Krishna Tirthaji Maharaja in the form of book Vedic M Ancient Indian.

Vedic Mathematics sutras, Urdhva Triyagbhyam or Vertically and Crosswise Algorithm for multiplication is discussed and then used to develop digital multiplier architecture. For division, different division algorithms are studied, by comparing drawbacks and advantages of each algorithm, Nikhilam Algorithm based on vedic mathematics is modified according to need and then used.

## 2. Background Work

In [1] Surabhi Jain and Sandeep Saini presents a direct method of computing the discrete linear convolution, circular convolution and deconvolution. The approach is easy to learn because of the similarities to computing the multiplication of two numbers. The most significant aspect of the proposed method is the development of a multiplier and divider architecture based on Ancient Indian Vedic Mathematics sutras Urdhvatriyagbhyam and Nikhilam algorithm. The results show that the implementation of linear convolution and circular convolution using vedic mathematics is efficient in terms of area and speed compared to their implementation using conventional multiplier & divider architectures.In [2] Madhura Tilak presents a novel method of implementing linear convolution of two proposed method uses modified design approach by replacing the conventional multiplier by Vedic multiplier internally in the implementations. The proposed method is efficient in terms of computational speed, hardware resources and area significantly. The efficiency of the proposed algorithm is tested by simulations and comparisons with different design approaches.The proposed circuit is also modular, expandable and regular which provides flexibility. In [3] Mrs.Rashmi Rahul Kulkarni ,convolution is carried out by serial processing. They used only one 4×4 bit Vedic multiplier based on Urdhva Tiryagbhyam sutra. Though hardware is less, delay is more as sixteen multiplications are carried out one by one using only single multiplier. In this paper, convolution of two finite length sequences is computed using Direct method. This method is similar to the multiplication of two decimal numbers, this similarity that makes this method easy to learn and quick to compute. As Vedic multiplier is high speed multiplier among existing multipliers, Urdhva Tiryagbhyam algorithm from Vedic mathematics is used for 4×4 bit multiplication and to improve speed parallel processing approach is used. In [4] Rashmi K. Lomte (Mrs.Rashmi R.

Kulkarni), Prof.Bhaskar P.C proposed deconvolution of two finite length sequences (NXM) using direct method to reduce deconvolution processing time. In this paper, we presented an optimized implementation of deconvolution. This particular model has the advantage of being fine tuned for signal processing. To accurately analyze our proposed system, we have coded our design using the VHDL hardware description language and have synthesized it for FPGA products using ISE. The proposed circuit uses less area and less power.

## 3. System Description

System describes, Vedic mathematics sutra urdhva triyagbhayam and nikhilam algorithm. Vedic Mutiplier:Urdhva Triyagbhyam: Among all available multipliers, this paper proposes a systematic design methodology for fast and area efficient digit multiplier based on Vedic Mathematics. In the proposed convolution method

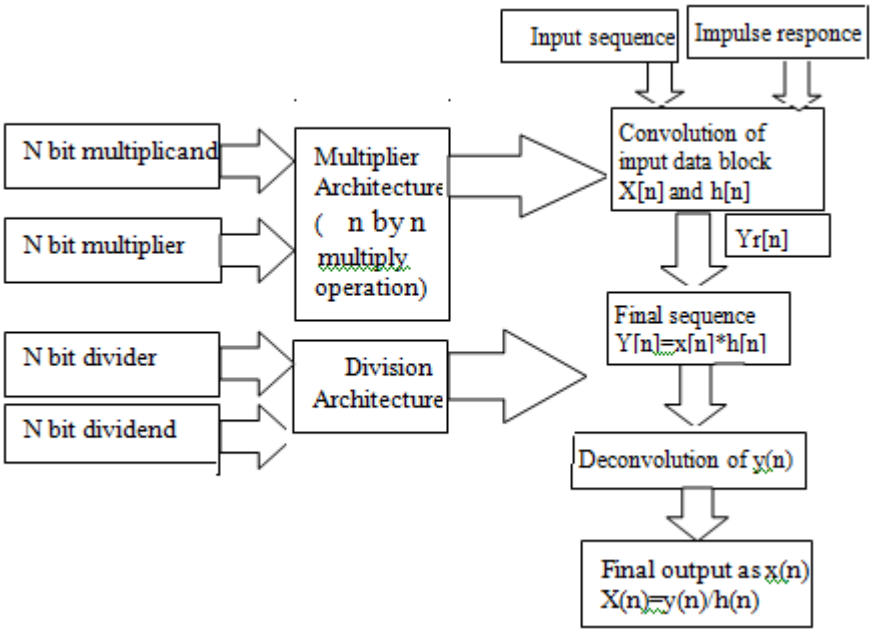


**Figure 1**

the multiplier architecture is based on an algorithm Urdhva Triyagbhyam (Vertical and Crosswise) of Ancient Indian Vedic Mathematics .The use of Vedic Mathematics lies in the fact that it reduces the typical calculations in conventional mathematics to very simple ones. Urdhva Tiryagbhyam Sutra is a general multiplication formula applicable to all cases of multiplication.In this paper, Urdhva-Tiryakbhyam Sutra is first applied to the binary number system and is used to develop digital multiplier architecture. This Sutra also shows the effectiveness of reducing the N×N multiplier structure into an efficient 4×4 multiplier structures. This work presents a systematic design methodology for fast and area efficient digital multiplier based on Vedic mathematics.The basic work proposed in this paper is been explained using the block diagram in Fig 1.Because of parallelism in generation of partial products and their summation obtained, speed is improved. For higher no. of bits in input, little modification is required. Divide the no. of bit in the inputs equally in two parts.

Vedic Divider: Nikhilam Algorithm: Nikhilam Navatascaramam Dasatah, literally meaning all from 9 And the last from 10. Deconvolution operation is implemented by using Nikhilam algorithm based on vedic mathematics while to obtain partial products vedic multiplier is used. In this paper, the block convolution and deconvolution algorithm is implemented in VHDL (Very High Speed Integrated Circuited Hardware Description Language) and the FPGA synthesis and logic simulation are done using quartus 2.

## 4. Conclusion

The main focus of this paper is to introduce a method for calculating the linear convolution, circular convolution and deconvolution with the help of vedic algorithms that is easy to learn and perform. The execution time and area of the proposed method for convolution using vedic multiplication algorithm is compared with that of convolution with the simple multiplication is less. From the simulated results it is observed that delay of Linear Convolution architecture is reduced by approximately 88% than the conventional method. An extension of the proposed linear convolution approach to circular convolution using vedic multiplier is also introduced which has less delay and area than the conventional method. This paper also introduced a straightforward approach to performing the deconvolution.

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