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VLSI Implementation for BIST Controller using Signed and Unsigned Multiplier

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Abstract: ***This journal mainly depicts the design and implementation of BIST (Built- in-Self-Test) using signed and unsigned multiplier. Power efficient in VLSI circuits is increasing day by day as rising demand of smart phones & Laptops. The present Modified Booth Encoding (MBE) multiplier and the Baugh-Wooley multiplier perform multiplication operation on signed numbers only. These two array multiplier and Braun array multipliers perform operations of multiplication on unsigned numbers only. But these days the main requirement of the modern computer system is a dedicated and very high speed unique multiplier unit for signed and unsigned numbers. Therefore, the main objective of this paper presentation is the design and implementation of SUMBE multiplier. By extending sign bit of the operands and generating an additional partial product the SUMBE multiplier is obtained. The Baugh-Wooley (BW) multiplier calculation is a for the most part doing direct with the assistance of marked augmentations. BIST Controller is circuit plans method in which parts of a circuit are utilized to test and check the obliged circuit. BIST Controller is for the most part a limited state machine in which state move is controlled by the Test Mode (TM) information. LFSR is a linear feedback shift register whose input bit is a linear function of previous function that contains the signal through the register from one bit to the next most-significant.***

Keyword: BIST, MBE, LFSR, Baugh-wooley multiplier, Booth multiplier

1. Introduction

Producing systems for VLSI circuits are most paramount and fabulous. So they can keep up a few issues that present in VLSI circuits. It is however immoderate to the clients in distinguishing if the delivered part is working legitimately or not. In this way, it is critical undertaking to test incorporated circuits (Ics) before shopping them. VLSI circuits are tried by giving distinctive test examples to the circuit under test (CUT) and contrasting the aftereffects of the circuit with the great circuit reaction. Realization process of VLSI technology can be explained as from basic needs that is what we want to do. This step arises through the basic needs of the customer and developer. First of all we must thought about customer‘s need or we must think about market situation.

The linear feedback shift register (LFSR) is that type of shift register which using feedback, and modifies itself on each rising edge of the clock. The feedback creates the required value in the shift register to cycle through a set of special values. The following choice of a LFSR length, gate type, LFSR type, its maximum length logic, and tap positions allows the user to control the realization and feedback of the LFSR, which, results in, controls the patterns of recapitulate values will repeated through. The current Modified Booth Encoding (MBE) multiplier and the Baugh-Wooley multiplier fulfill augmentation work on marked numbers just. The exhibit multiplier and Braun show multipliers complete increase operation on unsigned numbers just. Subsequently, the determination of the advanced machine framework is a dedicated and fast interesting multiplier unit for marked and unsigned numbers. Along these lines, this paper portrays the configuration and usage of SUMBE multiplier. This obliged changed Booth Encoder circuit delivers a large portion of the halfway items in parallel. By spreading sign bit of the operands and creating an extra fractional item the SUMBE multiplier is procured. The Carry Save Adder (CSA) tree and the last Carry Look ahead (CLA) viper are basically used to accelerate the multiplier method. Since marked and unsigned augmentation operation is finished by the same multiplier unit the obliged equipment and the chip operation range are lessens and along these lines this thusly abatements power dissemination and expense of a framework.

2. BIST (Built In-Self Test)

Bits controller is the main module in the required thesis which performs the bist function. It is like a state machine which used performing transition state from one state to another state. The State machine mainly consists of six states, (start, setmisr, resetmisr, test, hold and Bistdone). The limited state machine in which move state is controlled by the Test Mode (Test) info. It likewise gives the clock sign to the test example generator (LFSR), Circuit under Test (CUT) and the mark era circuit (Misr) in test state MISR manipulates different types of signatures. After calculation of the seven clock pulses the MISR output is captured and calculated outputs is compared with the Signature register. BIST controller is the main module in this dissertation which is the management of the bist functions. It is like a state machine used for state transition from one state to the other state.

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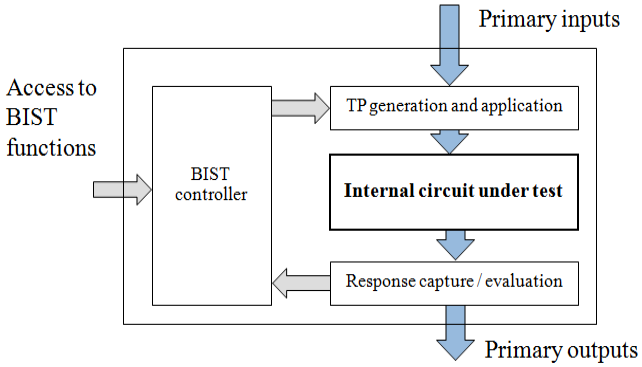

Figure 1: Architecture of BIST Controller

2.1 Principle of BIST

Above all else it produces test vectors, and afterward apply them to the circuit under test (CUT) or gadget under test (DUT), and after that confirm the reaction of yields. Figure demonstrates a basic BIST piece graph which utilizes a direct input movement register (LFSR) to deliver the test vectors and numerous information mark register (MISR) to confirm the yield against the right successions of the circuit under test.

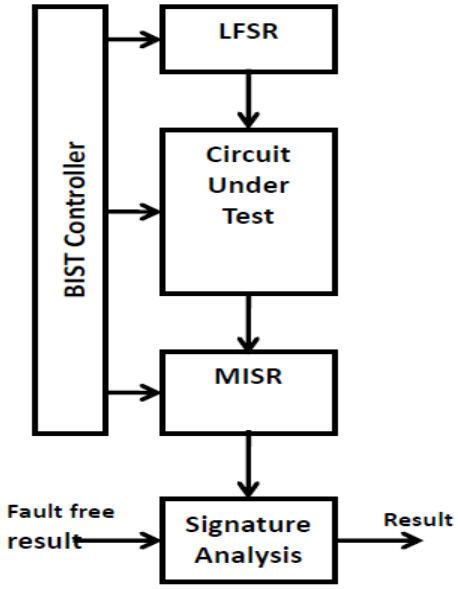

Figure 2: BIST Structure

BIST is a situated of organized test methodology for combinational and consecutive rationale, memories, Multipliers, and various other installed rationale squares. BIST is the regularly utilized configuration approach that allows a circuit to test inside itself. CUT (Circuit under Test) selector is used to select a cut out of three cut's in which the bist functions is performed. CUT is mainly a Multiplexer which has a two bit selection lines.

3. Linear Feedback Shift Register (LFSR)

In computing, LFSR is a linear feedback shift register whose input bit is a linear function of previous function that contains the signal through the register from one bit to the next most-significant when it is clocked as shown in figure.

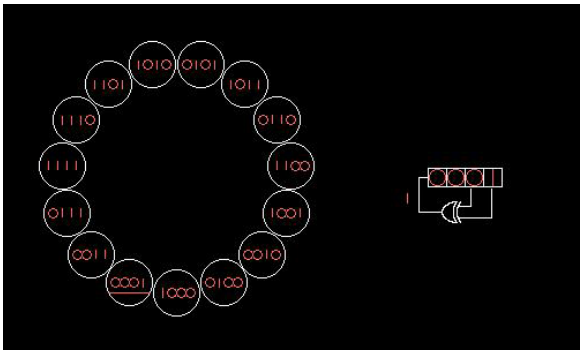

Figure 3: Fibonacci LFSR

A complete linear feedback shift register can be made simple by performing exclusive-OR gate on the outputs of two or more of the flip-flops and feeding those outputs back into the input of one of the flip-flops as shown in Figure. So an LFSR is a shift register whose input bit is driven by XOR gates of the overall shift register value. Linear feedback shift registers generates extremely good pseudorandom pattern generators. The initial value of a LFSR is called SEED, and because of its register operation is deterministic the extreme value generates by resister is completely depends on its currents as well as its previous states. It must eventually enter a repeating state because its resister has a finite number of possible states. However an LFSR with a feedback function generate a sequence of a bit which appeared random and has a very long cycle. Linear Feedback Shift Registers (LFSRs) are the fundamental instruments of many running keys generators components such as for stream cipher applications, because they are mostly applicable for hardware implementation and they also generates sequences with good fundamental properties.

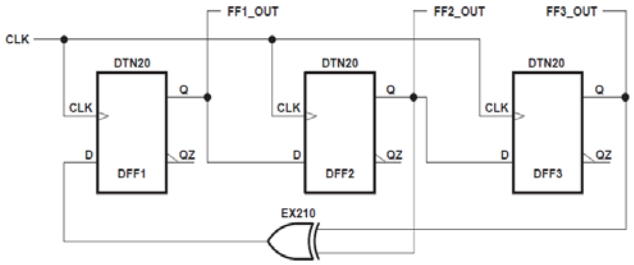

Figure 4: Linear Feedback Shift Registe

Table 1. Pattern-Generator Seed Values

CLOCK PULSE	FF1_OUT	FF2_OUT	FF3_OUT	COMMENTS
1	1	1	1	Seed value
2	0	1	1	
3	0	0	1	
4	1	0	0	
5	0	1	0	
6	1	0	1	
7	1	1	0	
8	1	1	1	Starts repeat

A maximum-length LFSR generates the maximum number of PRPG sequences possible and these are equal to 2n – 1 number of patterns, where n is the number of register components in the LFSR.

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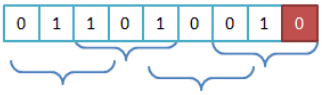
INPUTS					OUTPUTS		
CLOCK PULSE	A_IN	B_IN	C_IN		FF1_OUT	FF2_OUT	FF3_OUT
				SEED VALUE	1	0	0
1	1	1	1		1	0	1
2	0	1	1		1	0	1
3	0	0	1		1	1	1
4	1	0	0		1	1	1
5	0	1	0		0	0	1
6	1	0	1		0	0	1
7	1	1	0		0	1	0
8	1	1	1		0	1	0

The Parallel Signal Analyzer table

4. Booth Multiplier

The current Modified Booth Encoding (MBE) multiplier and the Baugh-Wooley multiplier fulfill augmentation work on marked numbers just. The exhibit multiplier and Braun show multipliers complete increase operation on unsigned numbers just. Subsequently, the determination of the advanced machine framework is a dedicated and fast interesting multiplier unit for marked and unsigned numbers. Along these lines, this paper portrays the configuration and usage of SUMBE multiplier. This obliged changed Booth Encoder circuit delivers a large portion of the halfway items in parallel. By spreading sign bit of the operands and creating an extra fractional item the SUMBE multiplier is procured. The Carry Save Adder (CSA) tree and the last Carry Look ahead (CLA) viper are basically used to accelerate the multiplier method. Since marked and unsigned augmentation operation is finished by the same multiplier unit the obliged equipment and the chip operation range are lessens and along these lines this thusly abatements power dissemination and expense of a framework.



Groups			Coding
0	1	0	1 × Y
1	0	0	-2 × Y
1	0	1	-1 × Y
0	1	1	2 × Y

X_{i+1}	X_i	X_{i-1}	Action
0	0	0	0 × Y
0	0	1	1 × Y
0	1	0	1 × Y
0	1	1	2 × Y
1	0	0	-2 × Y
1	0	1	-1 × Y
1	1	0	-1 × Y
1	1	1	0 × Y

Figure 5: Modified booth multiplier

4.1 An 8-bit Baugh-Wolley multiplication

The Baugh-Wooley (BW) multiplier calculation is a for the most part doing direct with the assistance of marked augmentations. Figure beneath speaks to the calculation for a 8-bit limb wolley multiplier, where the bits of the Partial-item results have been orchestrated. The plan of the obliged fractional item show comprises of principally three steps

(1) The most noteworthy bit (MSB) of the $N - 1$ halfway item columns and section of all bits of the last incomplete item push.
(2) The last result is transformed from the Least Significant Bit (LSB). The general deferral of the obliged multiplier can be chiefly isolated into three sections.
(3) The expansion of "1" is to include the Nth segment.

From these, the fundamental parts of the multiplier postponement are a direct result of the PPST and the last snake and the deferral because of the PPG is little. Thus, an imperative change in the velocity of the multiplier can be controlled by minimizing the proper postpone

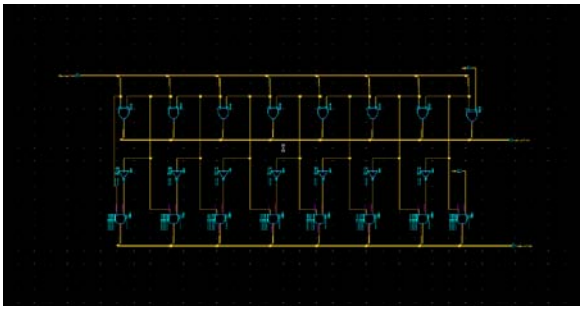


Figure 6: Circuit analysis of Booth Encoder

Now proposed work of 32-b MBE multiplie.

It can be noted that there is just 4.3%correctionoccured in the rate for 16-bit and 11.5% for 64-bit size. This obliged pace limit is happened in lower bit size multipliers due to the extensive distinction between info entry profile to the last CPA from those of part0 and part1. Presently with the incensement in the expression measure, the obliged contrast we got gets to be littler and the change in the velocity of the parceled multipliers bigger. It portrayed the remedied execution of the proposed systems and demonstrates that some piece of the zone of the apportioned multipliers with crossover CPA in which the greatest region of 5.7% is higher than those of the unpartitioned multipliers with CLA in 16-bit word size. Presently expanding of word size, the region overhead minimizes.

Conséquent it is clear that demonstrated in the assume that the range overhead of the propose strategies routinely minimizes with expanding word estimate and is just 0.6% overhead and 3.9%, 3.1% change if there should be an occurrence of 64-bit

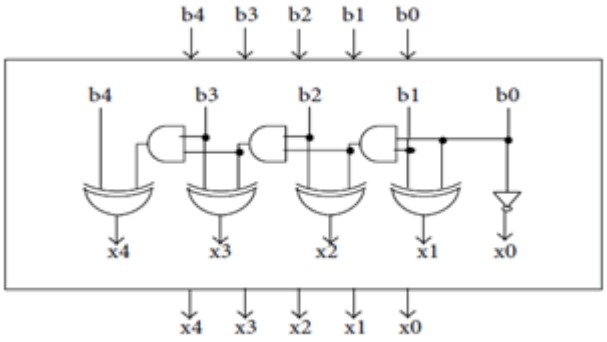


Table 2: Result of 32-bit multiplier

Word size	Multiplier	Delay (ns)	Area (μm^2)	Power (μW)
32	Regular	2.39	14,966	5.06
	Proposed	2.19	15,721	5.58

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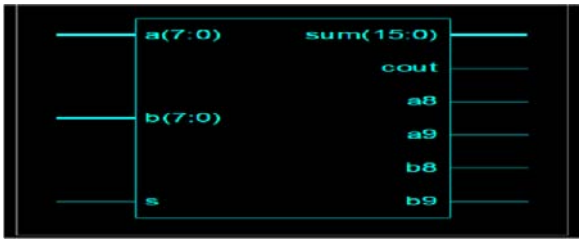

Figure 7: RTL view of 8×8 signed-unsigned multiplier

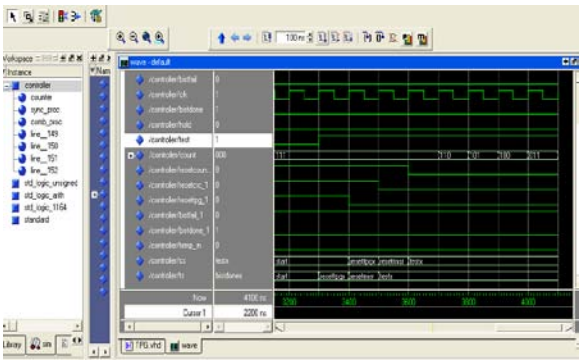

Figure 8: simulation for 8x8 multiplier

5. Results and Comparison

Verilog code is written to generate the required hardware and to produce the partial product, for CSA adder, and CLA adder. After the successful compilation the RTL view generated is shown in Fig.

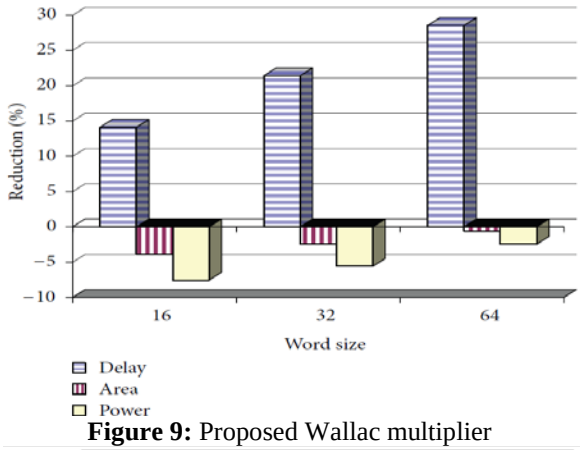

Figure 9: Proposed Wallac multiplier

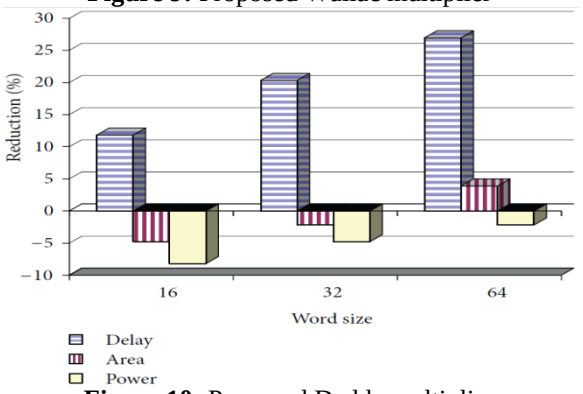

Figure 10: Proposed Dadda multiplier

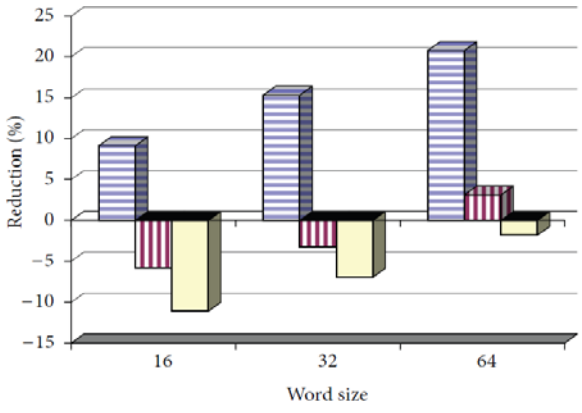

Figure 11: Proposed HTM multiplier

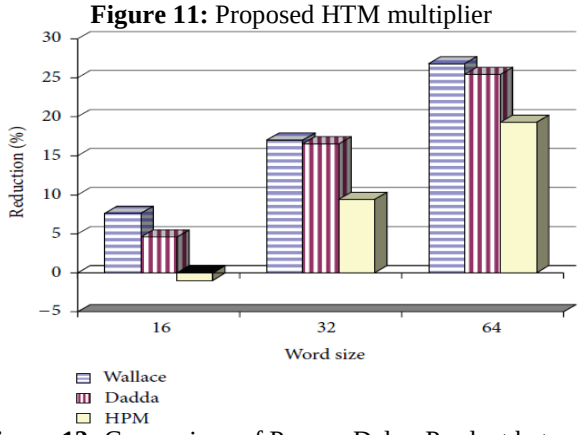

Figure 12: Comparison of Power- Delay-Product between Wallac, Dadda and HPM multiplier

6. Conclusion

A new memory Built-in Self-test and Repair conception has been implemented and this conception is suggested without using any extra rows and columns. This type of test and repair are only concentrated on the conformation of the memory addresses, this means there is no extra spaces required as the previous researches. The projected VHDL design in the LFSR of BIST in thesis, it will be asserted that the power of the LFSR is concentrated. By using minimum power LFSR proficiency, we can mention that the power in BIST implementation can be further decreased.

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References

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