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An Efficient Design for Reduction of Power Dissipation in Johnson Counter using Clock Gating

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Abstract: ***In this paper, a new method for minimizing power dissipation in 4-bit Johnson up-down counter is proposed. In this design, we have used a dual dynamic pulsed flip-flop (DDFF) [1], which supports embedding a logic module (DDFF-ELM) and a power saving technique, namely, clock gating [2] is used. We have used DDFF because it is power efficient compared to other flip-flops in the literature. We have used digital schematic editor (DSCH) for designing; simulation and layout generation is done using Microwind. From the simulation results, it is observed that power dissipation is reduced by 33.9 %.***

Keywords: Johnson counter, DDFF-ELM, DSCH, Microwind, clock gating

1. Introduction

Low power circuit design has become one of the main concerns in VLSI circuits now-a-days. As the size of chip reduces and speed increases, power dissipation has be-come an important designing parameter. Low power circuit design includes minimum number of logic gates and elimination of redundant operations.

In a digital system, all arithmetic, logic and memory op-erations will be performed synchronously according to the system clock. Therefore, efficient design of these sequen-tial circuits is very important. Counters and registers are the main sequential circuits that are used frequently in these digital systems. To perform different kinds of op-erations in these digital systems, different data sequences are required, so, different kinds of counters have to be designed. A Johnson counter is one of such, which will generate a particular data sequence, which will be used in many applications. In this paper, we have proposed a new design for reducing the power dissipation in a 4-bit Johnson up-down counter using DDFF-ELM flip-flop and clock gating technique.

Clock gating [2-5] is an efficient technique for reducing dynamic power dissipation in VLSI sequential circuits, it was first used by Intel in its Pentium-IV processor. It is observed that clock transitions consume a lot of power (almost 15-45%) in a digital system. Clock gating re-duces these unwanted transitions by adding more logic to a circuit to prune the clock tree. This leads to disabling certain portions of the circuit and so that flip-flops in that part need not to change their state, which saves a lot of power. So, power dissipation can be reduced by avoiding unnecessary clock pulses in a digital system. In this paper, clock gating system is implemented by using XOR and NAND gates.

In this paper, we have used DSCH and Microwind for the implementation and evaluation of the proposed de-sign. In DSCH a hierarchical digital circuit can be built and simulated. The main advantages of DSCH are: (i) a user friendly environment for rapid designing of logic circuits (ii) a built-in extractor which generates a SPICE net list from the designed schematic diagram (iii) generates a VERILOG description le of the schematic for layout conversion (iv) sub-micron, deep-submicron and Nano-scale technology support. Micro wind is a tool for designing and simulating circuits at layout level. The tool features full editing facilities, various views and an analog simulator. Microwind supports entire front end and back end design flow. For front end designing we have DSCH which possess inbuilt pattern based simulator for digital circuits. The back end design of circuits is sup-ported by Microwind. User can design digital circuit and compile here using Verilog le. Microwind automatically generates an error free CMOS layout. The CMOS layouts can be verified using inbuilt mix-signal simulator and analysed further for DRC and cross talk delays.

2. Literature Survey

Several flip-flops have been proposed in the past few decades, to improve speed and performance. Flip-flops are classified into two types: static and dynamic. In static flip-flops, the previous stored values will not be erased, even when the clock is removed. Some examples of static design are transmission gate latch based master slave flip-flop (TGMS) and PowerPc 603 master slave latch. The advantages of TGMS flip-flop are small area and only few internal nodes have to be charged and discharged during the absence of precharged. TGMS has its applications

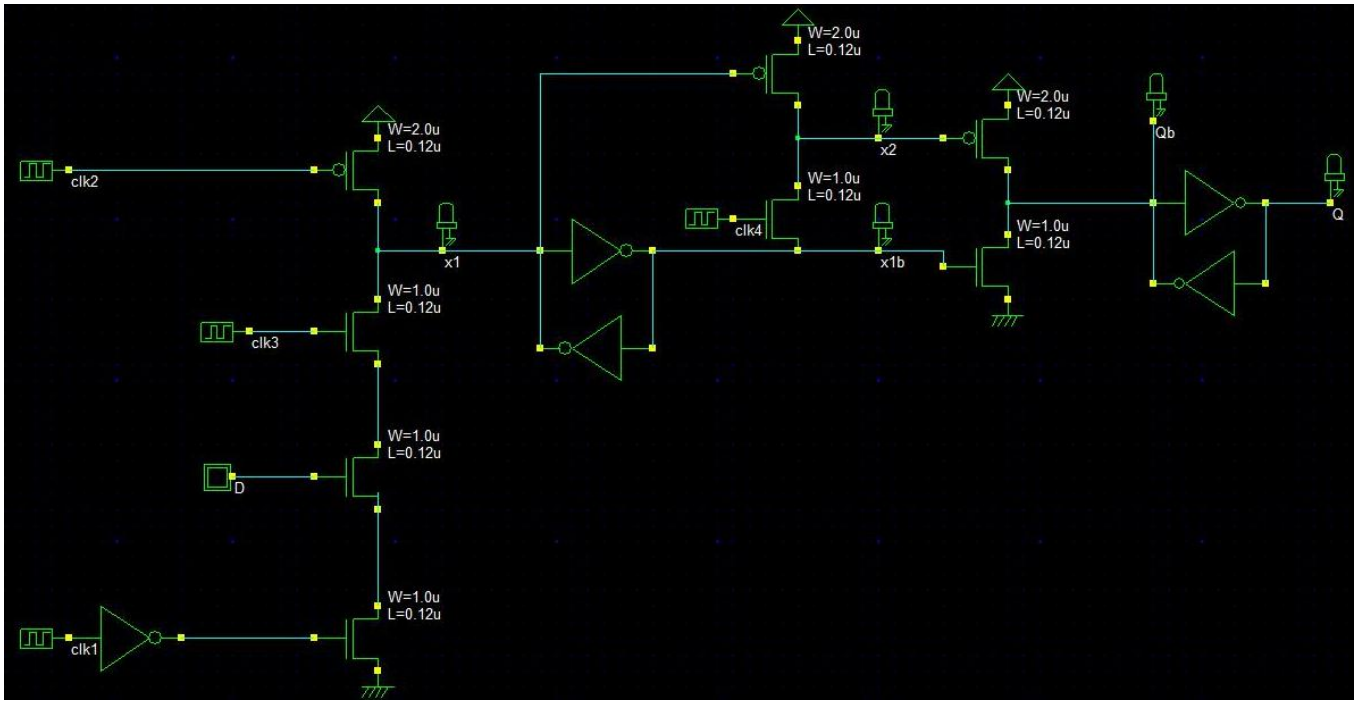

Figure 1: DDFF

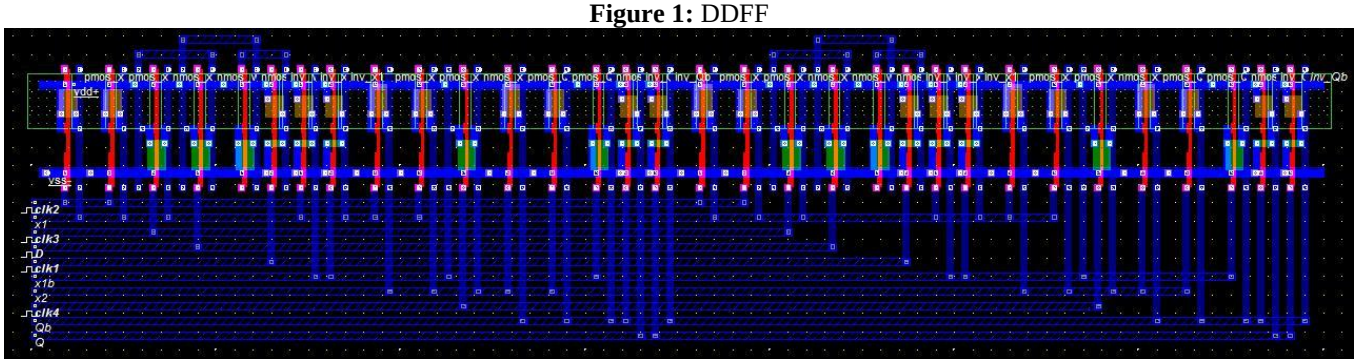

Figure 2: Layout design of DDFF

In energy efficient microprocessors. PowerPc 603 is the fastest flip-flop and its advantages are short direct path and low power feedback. The advantages of static de-sign are low power dissipation and low clock to output delay (CLK-Q) delay. The disadvantages include large positive setup time and large data to output delay makes unfit for some applications. Static designs are used when speed is not a major concern. Dynamic flip-flops are also called as modern high performance flip-flops. They can be purely dynamic or pseudo dynamic. Semi dynamic flip-flop (SDFF) [7] and hybrid latch flip-flop (HLFF) [6] fall under this category. SDFF is one of the high performance flip-flops based on hybrid mechanism. Its features include small delay, logic embedding, small size and simple topology, but it is not suitable in low power applications. In SDFF, it is observed that considerable portion of power is dissipated due to unnecessary transitions that results in glitches, which results in high power dissipation. HLFF works similar to standard flip-flops in that it samples data on one edge of clock and eliminates retards flow in other edge. Both SDFF and HLFF perform latching operation by making use of clock overlap. Since, HLFF has longer stack of nmos transistors at the output, it has low power consumption, but it is fastest. SDFF is the fastest but be-cause of large clock load and large precharge capacitance it is not good as far as power consumption is concerned. Power dissipation in the conventional designs is due to redundant data transitions and large precharge capaci-tance. The main intention of many flip-flop designs is to eliminate these two main problems. A conditional data mapping flip-flop (CDMFF) is efficient w.r.t. minimizing redundant operations. An output feedback structure con-ditionally feeds the data to flip-flop and thus eliminates the unwanted transitions in CDMFF. The drawbacks of this flip-flop are bulky in size (because of additional tran-sistors) and large power consumption at higher data ac-tivities. The main drawback present in the conventional designs is large precharge capacitance. This common drawback is considered in design of cross charge control flip-flop (XCFF) [8], where in the large precharge capaci-tance present in output node is eliminated by separately driving the output of pull up and pull down transistors. The total power consumption is reduced because only one dynamic node switches during a clock cycle. The draw

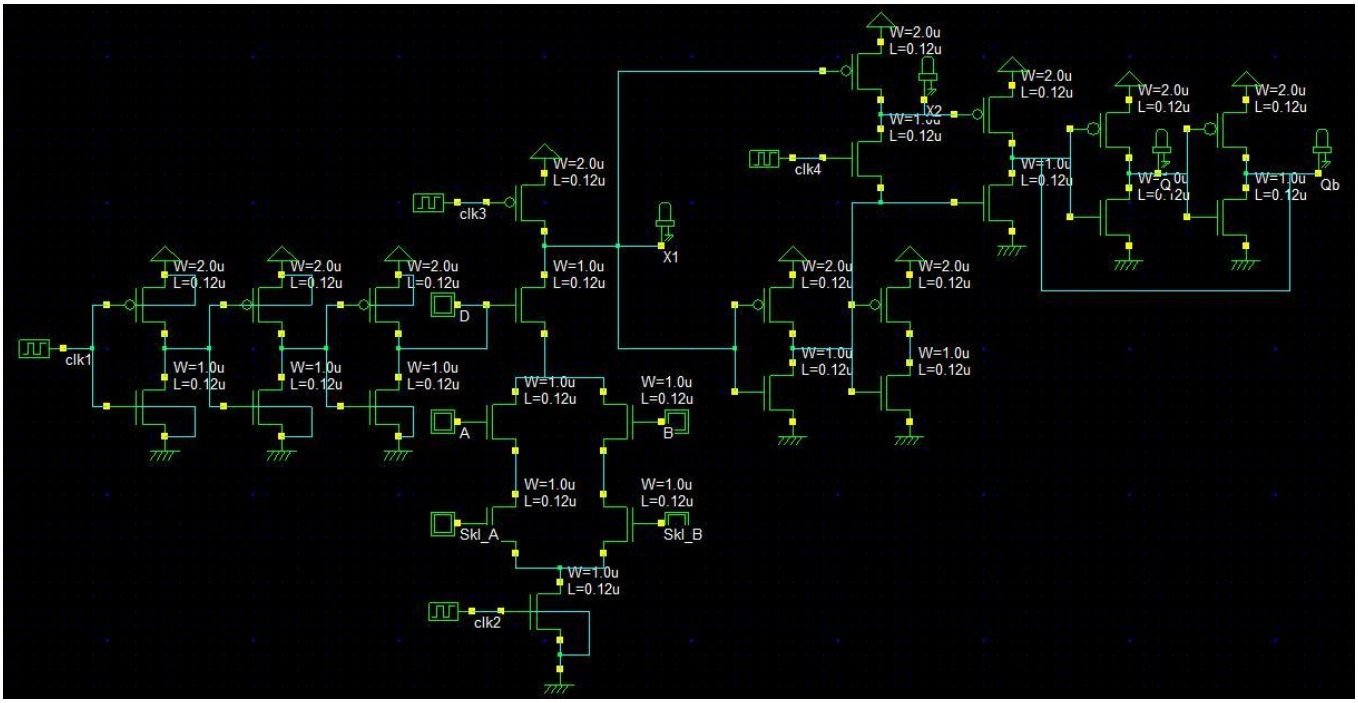

Figure 3: DDFF-ELM with 2-by-1 Multiplexer as embedding module

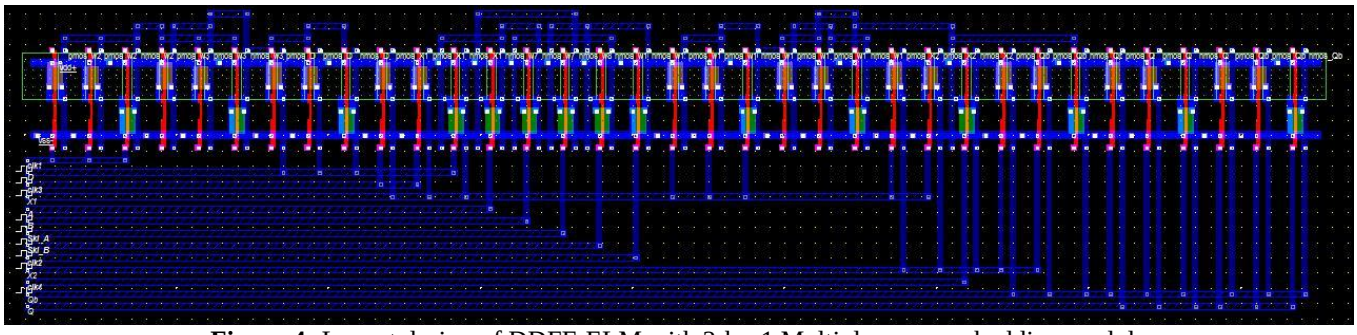

Figure 4: Layout design of DDFF-ELM with 2-by-1 Multiplexer as embedding module

backs of this design are conditional shut o mechanism and charge sharing, which is a serious problem in dynamic circuits. The effect of charge sharing is severe when complex functions are embedded in XCFF.

The drawbacks in XCFF are eliminated in DDFF by us-ing a split dynamic node structure which separately drives the output of pull up and pull down transistors, as shown in Figure 1. In DDFF architecture, node X1 is pseudo dynamic and node X2 is purely dynamic. Here an unconditional shut o mechanism is provided instead of conditional one as in XCFF. DDFF operation is divided into two phases: (i) evaluation phase (clock is high) and (ii) precharge phase (clock is low). The performance improvements indicates that it is well suited for modern applications where minimum delay and low power dissipation are required. Figure 2 shows the layout design of DDFF, generated using Microwind.

Figure 3 shows the architecture of DDFF with 2-by-1 multiplexer used as embedding module (DDFF-ELM) and Figure 4 shows its layout. The advantages of DDFF-ELM over other flip-flops (which has embedding logic capability) are lower power consumption and capability of embedding complex logic functions.

3. 4-Bit Johnson Up-Down Counter

Counters are frequently used in digital computers and other digital systems to record the number of events occurring in a specified interval of time. The counter should have memory to count the occurrences of events, so, counters are designed using flip-flops. There are different types of counters used in digital circuits. An up-down counter is a bidirectional counter and it has to be made to count upwards as well as down wards. Since the complemented output of last flip-flop is connected as input to the first flip-flop, it is called as twisted ring counter. The counting sequence repeats for every 8 clock cycles. Figure 5 shows the architecture of 4 bit Johnson up down counter. Figure 6 shows the schematic of 4-bit Johnson counter without clock gating implemented in DSCH. Figure 7 shows the layout of Figure 6 generated using Microwind.

In this paper, a Johnson up-down counter is designed by using DDFF-ELM by embedding a 2-by-1 multiplexer in the architecture of DDFF. We have studied the power dissipation of Johnson counter in the following two cases:

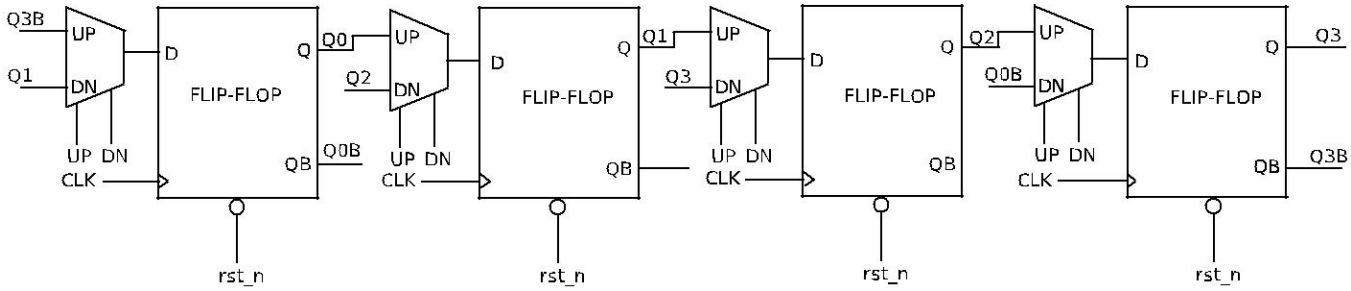

Figure 5: 4-bit Johnson up-down counter

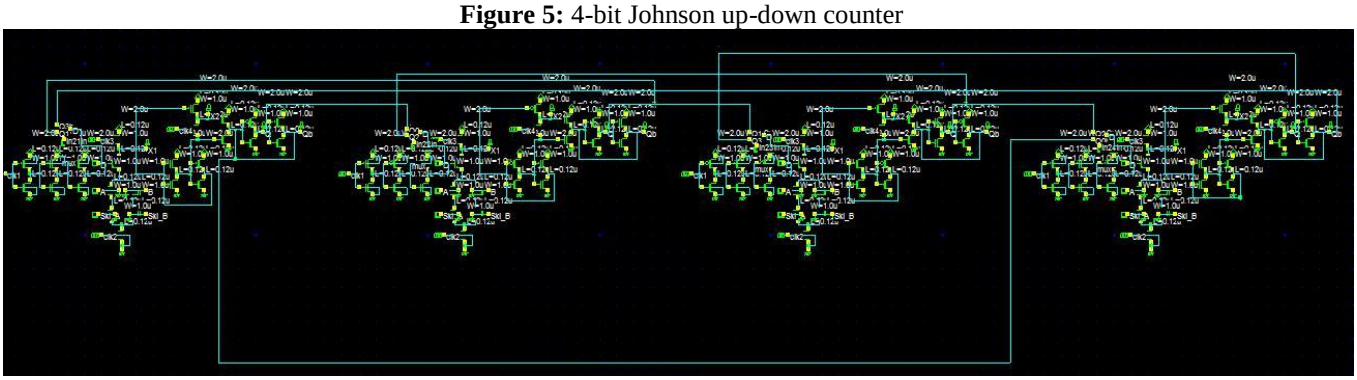

Figure 6: 4-bit Johnson up-down counter without clock gating

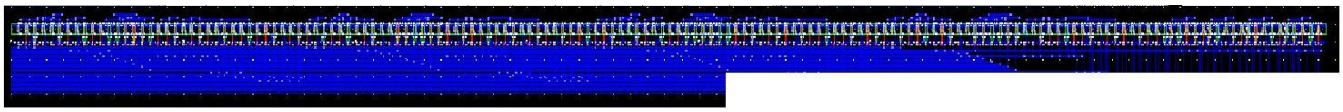

Figure 7: Layout of 4-bit Johnson up-down

(i) without clock gating and
(ii) with clock gating

4. Johnson Counter using Clock Gating

Clock gating is a power-saving technique used in the design of digital circuits. The main aim of this technique is to supress the unwanted clock transitions from propagating to the clock circuitry. Clock power contributes 50 to 70% of the total chip power and in the next gen erations it is going to increase drastically. So minimizing the power dissipation is very important in digital circuits. Each of the clock gating block uses XOR and NAND gate as shown in Figure 8. Figure 9 shows the block diagram of 4-bit Johnson up-down counter with clock gating technique applied. This is implemented in DSCH and Microwind as shown in Figures 10 and 11.

5. Simulation Results

The existing and proposed designs are implemented in Microwind software using 90 nm technology. Schematics for the design are designed in digital schematic editor (DSCH).the following are the timing diagrams for John-son counter without clock gating and Johnson counter with clock gating. Figures 12 and 13 shows the timing diagrams of Johnson counter without and with clock gating, respectively. From Table 1, we can observe that, power dissipation of 4-bit synchronous Johnson up down counter without clock gating is 11.14 mw, whereas, power dissipation of 4-bit synchronous Johnson up down counter by using clock gating is 7.36 mw. So the power consumption of the circuit decreases.

Table 1: Power dissipation of Johnson up down counter

Johnson counter	Power dissipation (mw)
without clock gating	11.14
with clock gating	7.36

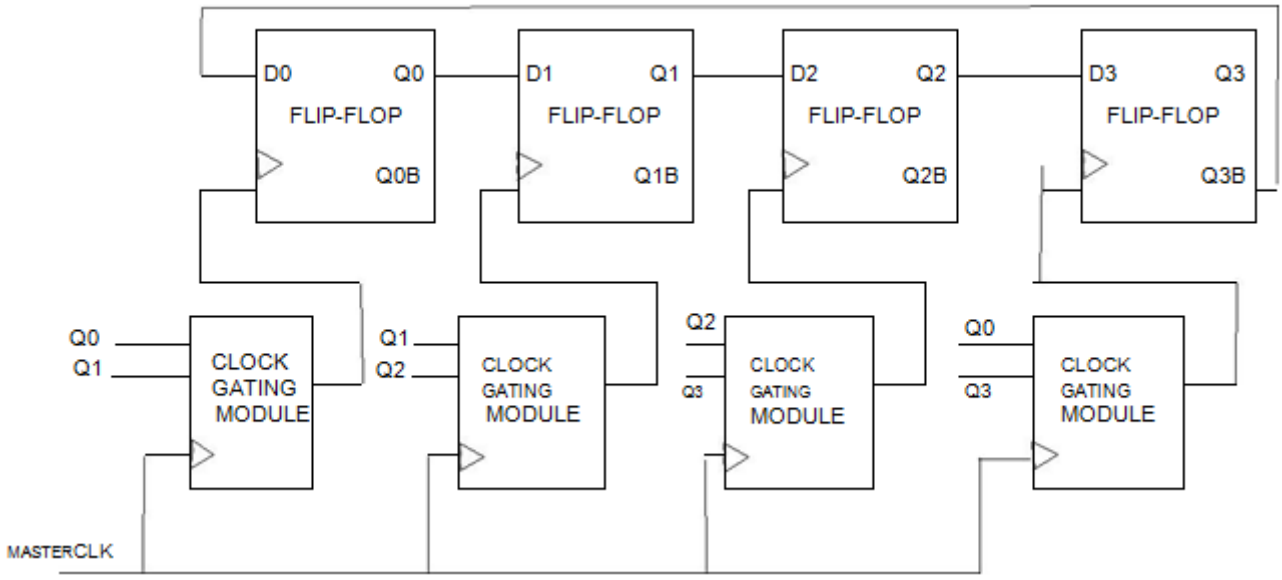

Figure 9: Block diagram of 4-bit up-down Johnson counter using clock gating

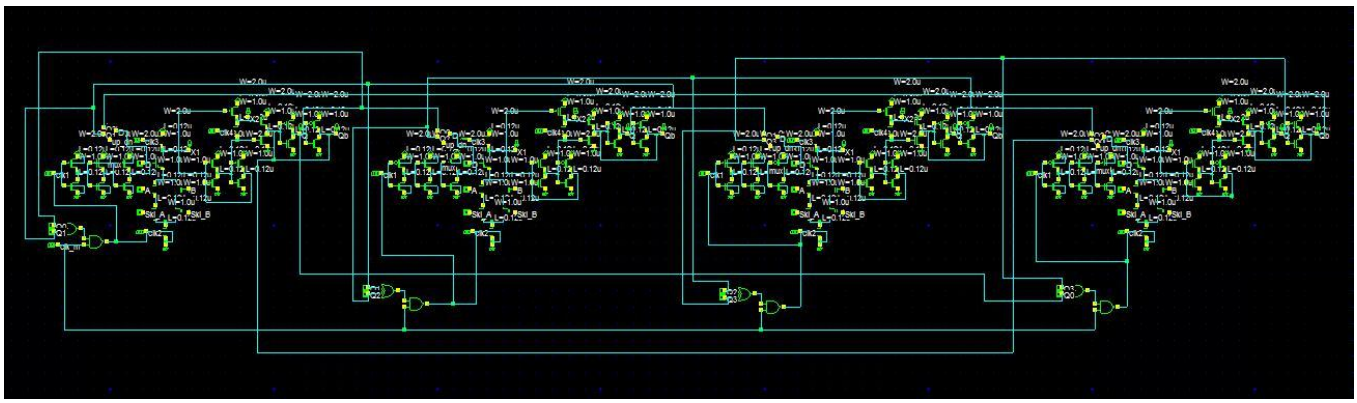

Figure 10: 4-bit Johnson up-down counter with DDFF-ELM and clock gating

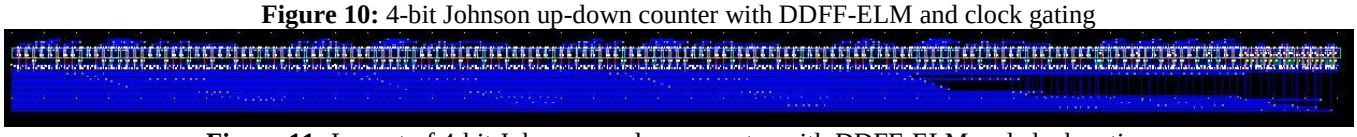

Figure 11: Layout of 4-bit Johnson up-down counter with DDFF-ELM and clock gating

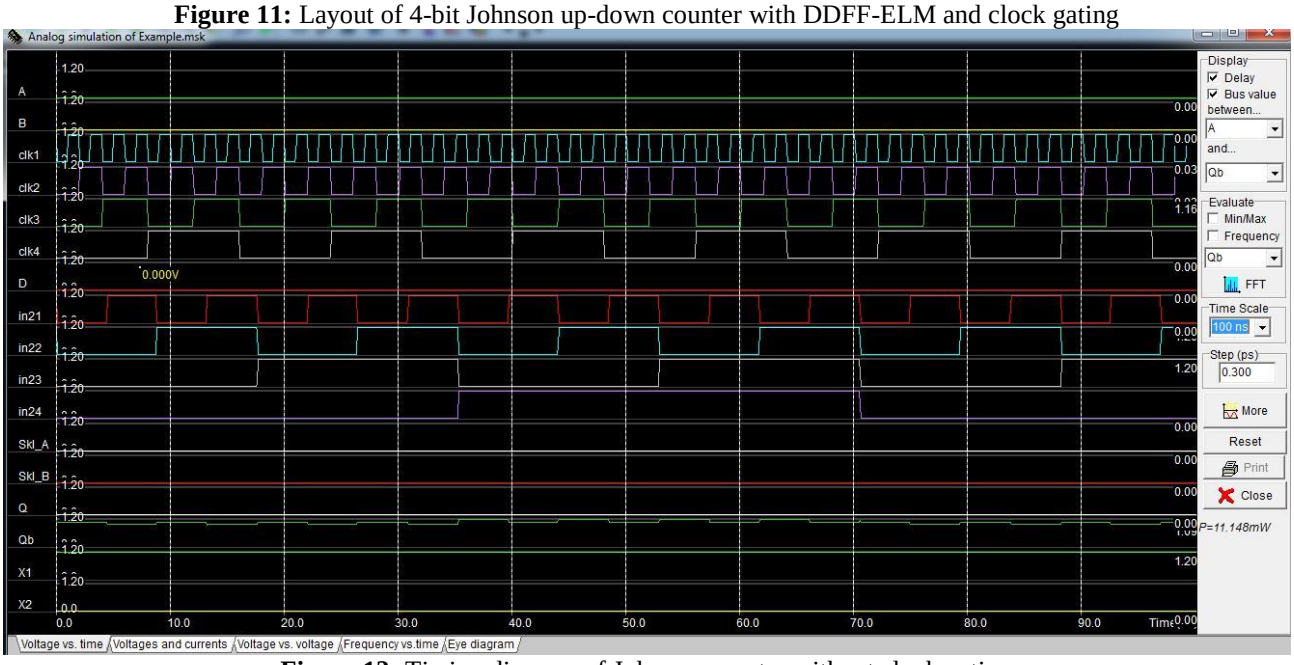

Figure 12: Timing diagram of Johnson counter without clock gating

Figure 13: Timing diagram of Johnson counter with clock gating

6. Conclusion

In this paper, we have proposed a power efficient design for 4-bit Johnson up-down counter, implemented using DDFF-ELM and clock gating. Simulation results shows that power dissipation of Johnson counter with clock gating is reduced by 33.9%, when compared with power dissipation of Johnson counter without clock gating. This design can be well used in all modern designs where power consumption is a main concern.

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