Table 3: Comparison of transistor count in 4-bit multiplier (array & tree) for various logic designs at different supply voltages in 180nm technology.

	CSL	CPL	DPL
Array Multiplier	432	384	528
	432	384	528
	432	384	528
Tree Multiplier	432	388	528
	432	388	528
	432	388	528

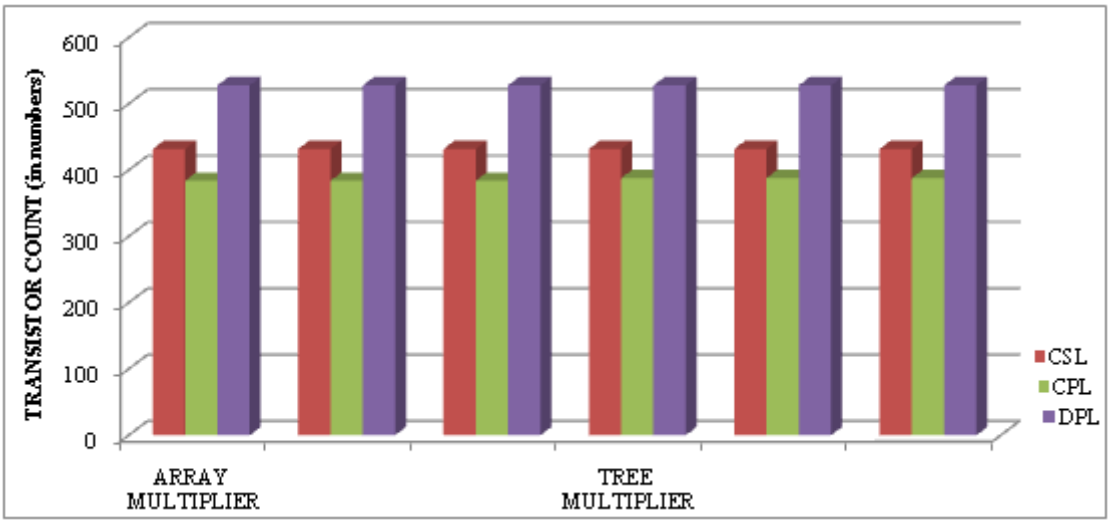

Figure 8: Comparison of transistor count in 4-bit multiplier (array & tree) for various logic designs at different supply voltages

Table 4: Power delay product (m-nj) comparison for different styles at 180nm technology

	CSL	CPL	DPL
ARRAY MULTIPLIER	0.19	0.37	0.13
	0.15	0.31	0.11
	0.12	0.30	0.10
TREE MULTIPLIER	0.17	0.49	0.14
	0.14	0.48	0.12
	0.12	0.45	0.10

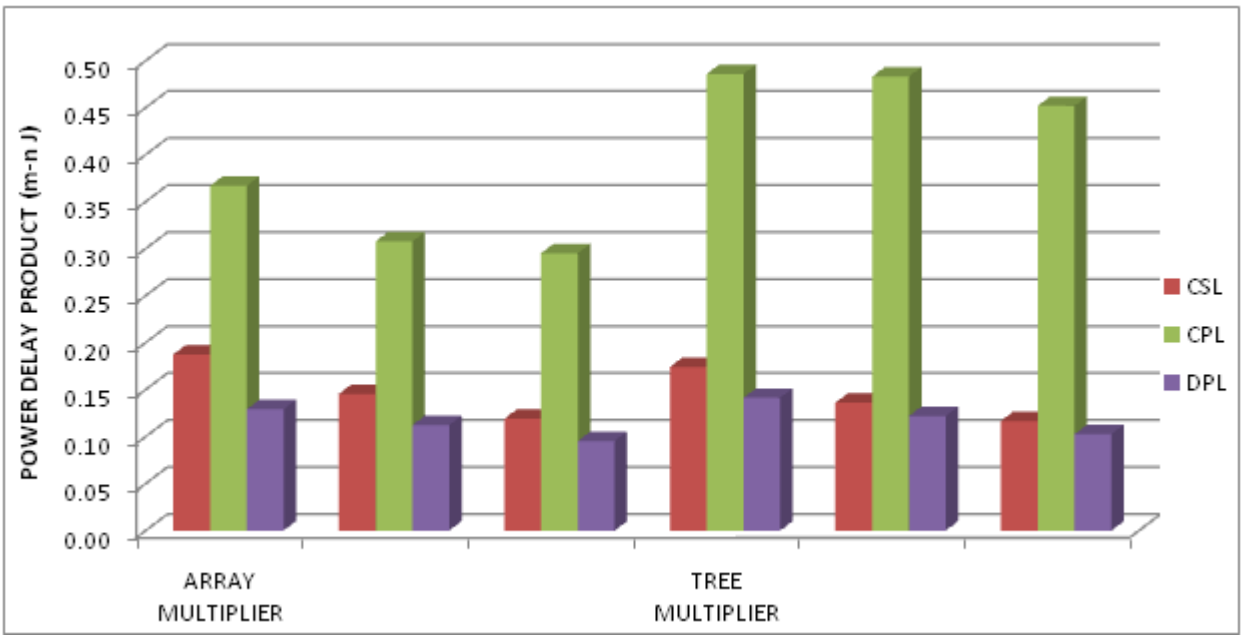

Figure 9: Power delay product (m-nj) comparison for different styles at 180nm

5.2 350nm technology at different supply voltages

Table 5: Comparison of Power Dissipation in 4-bit multiplier (array & tree) for various logic designs at different supply voltages in 350nm technology.

	CSL	CPL	DPL
ARRAY MULTIPLIER	2.87	16.64	12.38
	2.72	3.94	3.94
	2.51	3.46	3.46
TREE MULTIPLIER	2.86	19.60	19.60
	2.69	6.93	6.93
	2.49	6.42	6.42

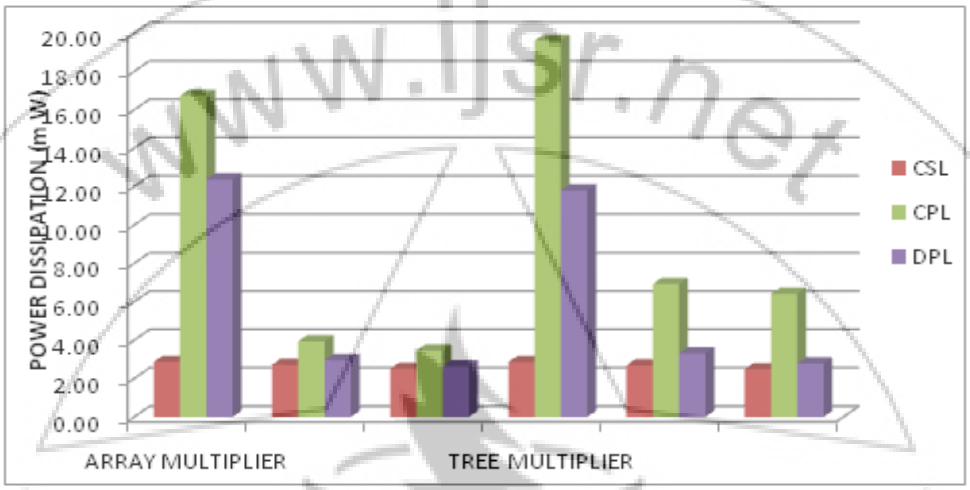

Figure 10: Comparison of Power Dissipation in 4-bit multiplier (array & tree) for various logic designs at different supply voltages

Table 6: Comparison of Propagation delay in 4-bit multiplier (array & tree) for various logic designs at different supply voltages in 350nm technology.

	CSL	*CPL*	*DPL*
ARRAY MULTIPLIER	0.675	0.607	0.530
	0.691	0.634	0.542
	0.943	0.639	0.570
TREE MULTIPLIER	0.605	0.707	0.525
	0.671	0.712	0.545
	0.688	0.765	0.550

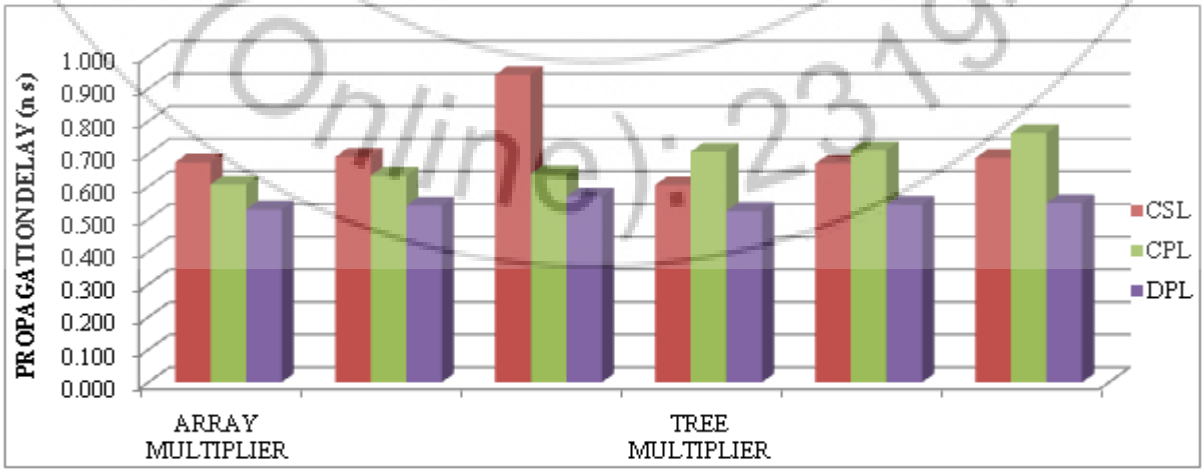

Figure 11: Comparison of Propagation delay in 4-bit multiplier (array & tree) for various logic designs at different supply voltages

Table 7: Comparison of transistor count in 4-bit multiplier (array & tree) for various logic designs at different supply voltages in 350nm technology.

	CSL	*CPL*	*DPL*
ARRAY MULTIPLIER	1.94	10.16	6.56
	1.88	2.50	1.60
	2.37	2.21	1.50
TREE MULTIPLIER	1.73	13.86	6.20
	.180	4.91	1.80
	1.71	4.93	1.53

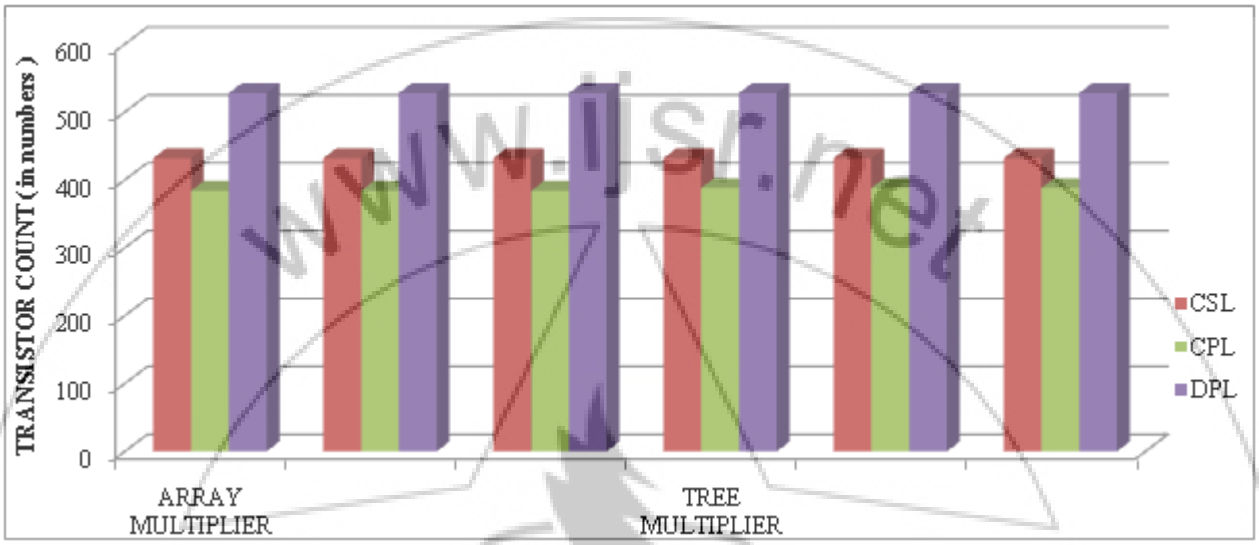

Figure 12: Comparison of transistor count in 4-bit multiplier (array & tree) for various logic designs at different supply voltages in 350nm technology.

Table 8: Power delay product (m-nj) comparison for different styles at 350nm

	CSL	CPL	DPL
Array Multiplier	432	384	528
	432	384	528
	432	384	528
Tree Multiplier	432	388	528
	432	388	528
	432	388	528

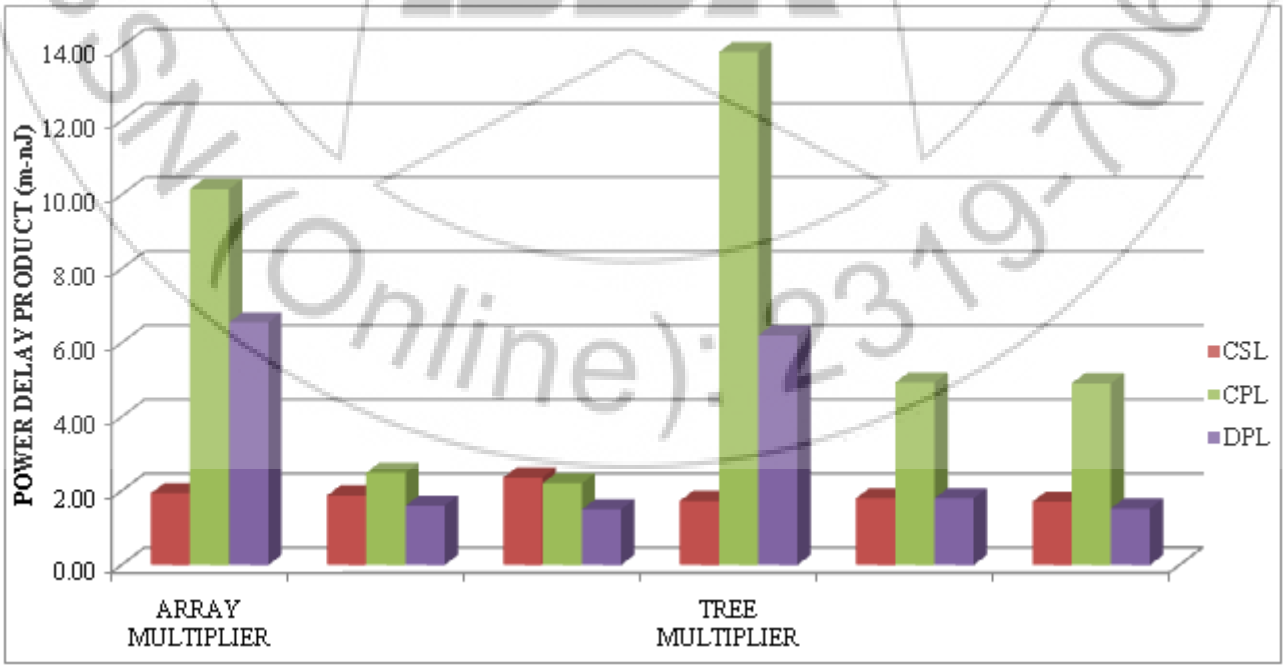

Figure 13: Power delay product (m-nj) comparison for different styles at 350nm

6. Conclusions

It is concluded from Power dissipation comparison that CSL has lowest power dissipation. DPL design style has higher power dissipation but very close to CSL. So it is better to design a system with CSL where low power dissipation is required like portable digital systems e.g. laptop. CPL logic style power dissipation is highest among all. From Propagation delay comparison that DPL design style has least propagation delay time than CSL and CPL. so it is better to use DPL logic style to design a system where fast speed is required. The CSL technique is slowest among all. It is concluded from number of transistors comparison that CPL technique requires less number of transistor to design a system than other two design styles. So electronics circuits designed using CPL logic style will occupy less space on the chip. DPL style has the lowest power- delay product than other two design styles. Thus DPL has the best performance in terms of speed and power dissipation at lower supply voltages. Overall comparison shows that Tree Multipliers are fast or have less propagation delay but consumes more power than Array Multiplier. Also as supply voltage is decreased, the power dissipation decreases and propagation delay increases.

7. Future Scope

Future work in this thesis may include a further scaling down of the technology. Hybrid architecture which is a mixture of Array & Tree architecture can be advised for the proposed multiplier so that speed can be increased and power dissipation can be decreased. To maximize the performance of multiplier 5 to 2 carry save adders can be used to sum the partial products as they are generated.

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References

[1] M.B. Damle, Dr. S.S Limaye and M.G. Sonwani, "Comparative Analysis of Array Multiplier Using Different Logic Styles", IOSR Journal of Engineering (IOSRJEN), Vol. 3, No. 5, pp. 16-22, May 2013.
[2] T. Sharma, Prof. B.P.Singh, K.G.Sharma, N. Arora , "High Speed Array Multipliers Based on 1-Bit Full Adders", in Int. J. of Recent Trends in Engineering and Technology, Vol. 4, No. 4, pp.26-28, Nov 2010.
[3] J.T.Yan and Z. W. Chen, "Low-power multiplier design with row and column bypassing", IEEE International SOC Conference, pp.227-230, 2009.
[4] Ming-Chen Wen, Sying-Jyan Wang, and Yen-Nan Lin ''Low Power Parallel Multiplier with Column Bypassing'' IEEE, 2005
[5] Chin-Long Wey and Ji-Fu Li ''Design of Reconfigurable Array Multipliers and Multiplier-Accumulators'' IEEE, 2004
[6] Dimitrios Soudris, Christian Piguet and Costas Goutis, "Designing CMOS Circuits for Low Power", Kluwer Academic Publisher, Boston, 2002
[7] B Parhami, "Computer Arithmetic – Algorithms and Hardware Designs", Oxford University Press, 2000.
[8] R Zimmermann and W Fichtner, "Low power logic styles : CMOS versus Pass Transistor Logic", IEEE Journal of Solid-State Circuits, Vol. 32, No. 7, pp. 1079-1090, July 1997.
[9] Tanner EDA Inc. 1988, User_s Manual, 2010.
[10] T. Kuroda et al., "Overview of Low-Power ULSI Circuit Techniques"
[11] Bellaouar, A., and Elmasry, M. I., Low-Power Digital VLSI Design: Circuits and Systems, Kluwer, Norwell, MA, 1995.
[12] Weste, and K. Eshraghian, "Principles of CMOS VLSI Design", Addison-Weslet Publishing Company, 1992
[13] C S Wallace, "A Suggestion for a Fast Multiplier", IEEE Transactions on Electronic Computers, EC-13, pp. 14-17, 1964.

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