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Design and Analysis of CMOS Multipliers at 180nm and 350nm

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Abstract: ***Due to rapid growth of portable electronic systems like laptop, calculator, mobile etc. and the low power devices have become very important in today world. Multiplier is the important arithmetic unit in Microprocessors and DSPs and also has a major source of power dissipation. To reduce the power dissipation is the important key to satisfy the power budget of various circuits. This paper elaborates the array multiplier and tree multiplier through different logic styles. In this the fundamental units to design a multiplier are adders. The various types of adders used in this paper are Complimentary Pass transistor Logic (CPL), Double Pass transistor Logic (DPL) and Conventional Static CMOS (CSL) Logic design styles using the 350nm and 180nm technologies at different supply voltages. The main objective of our work is to analysis the CMOS Multipliers in terms of Propagation delay and Power dissipation and Transistor count of 4x4 multipliers. The design of full adder for low power is obtained and the low power units are implemented on the array multiplier and tree multiplier and the results are analyzed for better performance. The designs are done with the help of TANNER S-EDIT tool and are simulated using T-SPICE***.

Keywords: Array Multipliers, Full adder, CMOS, CPL, DPL

1. Introduction

The high-speed and low-power very large scale integration can be implemented with different logic styles. The three most important methods to measure the quality of VLSI circuit is the area, power dissipation and time delay [1]. There are many logics for low power-dissipation and high speed. But each logic style has its own advantage in terms of power, time delay and layout implementation. In this paper, three Different types of logic styles are used to implement a 4-bit multiplier and then analyzed for power and speed Performance. The main goal is to find the right logic style for high speed and low power-dissipation. Multiplier is the necessary element of the digital signal and image/audio processing system such as filtering, convolution and inner products hence high speed is crucial to develop for real processing applications. Hence for real time multimedia applications the speed and power consumption are very important factors for good performance. This paper describes the implementation of a 4-bit multiplier using Complimentary Pass transistor Logic (CPL), Double Pass Transistor Logic (DPL) and Conventional Static CMOS (CSL) Logic styles using the 350nm and 180nm technologies.

2. Logic Styles

There are different designs for MAC such as superiors power suppression techniques (SPST), booth encoder etc. instead of these we follow the three techniques CSL, CPL and DPL for multiplier design

2.1 Conventional Static Logic (CSL)

Conventional static CMOS logic is used in most chip designs in VLSI applications. It consists of complementary NMOS pull-down and PMOS pull-up networks to drive '0' and '1' outputs. The features of this logic style are good noise margin, fast speed, low power and easy to design and the Other advantage of static CMOS logic style is its robustness against voltage scaling and transistor sizing which enables reliable operation at low voltages and arbitrary transistor sizes[8]. The circuit diagram is shown

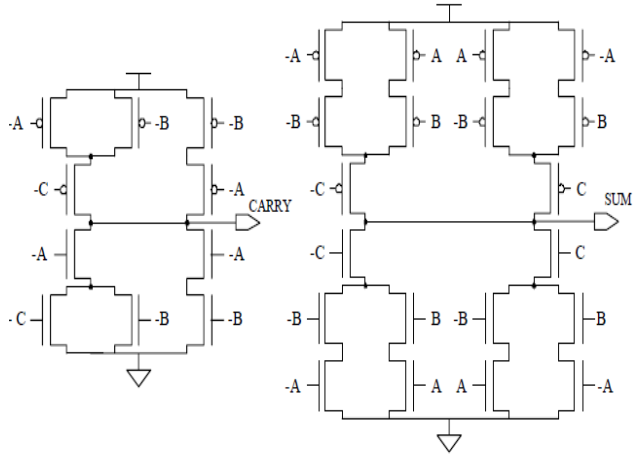

Figure 1: CSL Logic Full adder

2.2 Complementary Pass Transistor (CPL)

CPL consists of complementary inputs, outputs, an NMOS pass transistor logic network, and CMOS output inverters. As inverted and non-inverted inputs are needed to drive the gates of the pass-transistors, the complement of the logic also needs to exist which selects between the possible non-inverted output values which drives an inverter to generate an inverted version of the output. Since the high voltage level of the pass- transistor outputs is lower than the supply voltage level by the threshold voltage of the pass transistors,

$$V_{max} = V_{DD} - V_{T_n}$$

The signals have to be amplified by using the CMOS inverters at outputs [6]. The main concept behind CPL is the use of only an n-MOSFET network for the implementation of logic functions. The elimination of PMOS transistors form the pass-gate network reduces the parasitic capacitances associated with each node in the circuit so speed of operation increases. The circuit diagram of CPL is shown as

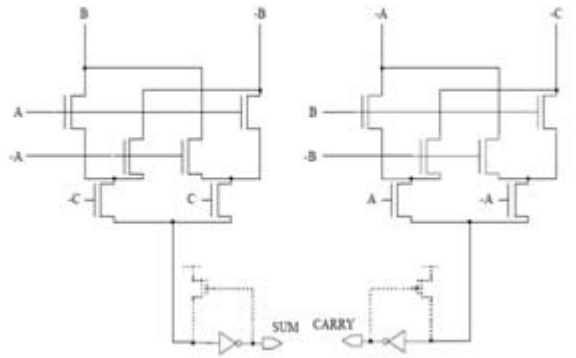

Figure 2: CPL Logic Full adder

2.3 Double Pass Transistor Logic (DPL)

The Double Pass transistor logic is a modified version of CPL. The DPL also has complimentary inputs and outputs and thus it is implemented using dual-rails. In DPL circuits, full voltage swing is achieved at outputs by adding a PMOS transistor in parallel with NMOS transistors. Although the addition of PMOS transistors results in increased capacitance compared to CPL style but this does not limit the performance of DPL because DPL gates have balanced input capacitance, thus reducing the dependence of delay on input data. The problems of noise margin and speed degradation in CPL circuits due to high reduced voltage level are solved out in DPL design style. The output buffers are not necessary, since the full swing is achieved by the addition of PMOS transistor. The circuit diagram of DPL is shown as

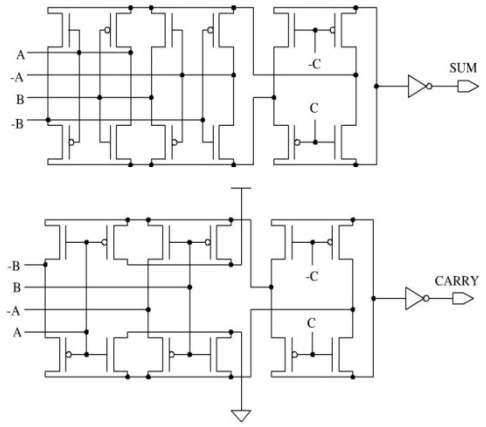

Figure 3: DPL Logic Full adder

3. Array Architecture

Array architecture based MAC uses short wires that go from one full adder to adjacent full adders horizontally, vertically or diagonally [7]. In array architecture based n × n bit multiplier uses array of AND gates can compute all the $a_i b_j$ terms simultaneously. The terms are summed by an array of 'n [n - 2]' full adders and 'n' half adders. The shifting of partial products for their proper alignment is performed by simple routing and does not require any logic. The advantage of array architecture is its regular structure. Thus it is easy to layout and has small size. The size of array architecture based multiplier increases in size at a rate equal to square of the multiplier operand size.

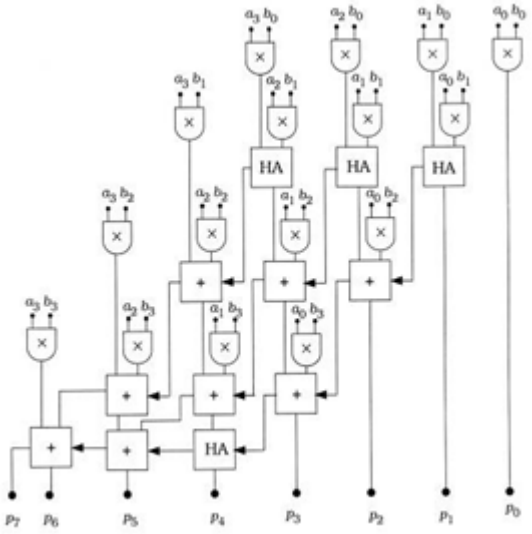

Figure 4: Array Architecture

4. Tree Architecture

C. S. Wallace suggested a fast technique to perform multiplication in 1964 [13]. The amount of hardware required to perform tree architecture based multiplication is large but the delay is near optimal. The partial products or multiples are generated simultaneously by using a collection of AND Gates. The multiples are added in combinational partial products reduction tree using carry save adders, which reduces them to two operands for the final addition. The results from CSA are in redundant form. Finally, the redundant result is converted into standard binary output at the bottom by the use of CPA. The advantage of tree multiplier is reduction in delay and it is given by log (N) where N is the length of multiplier or word length. Due to small no. of signal transitions, the power dissipation is reduced. The disadvantage of tree is its irregular structure. So these are difficult to design, layout and also require significant area. Wiring is more complex.

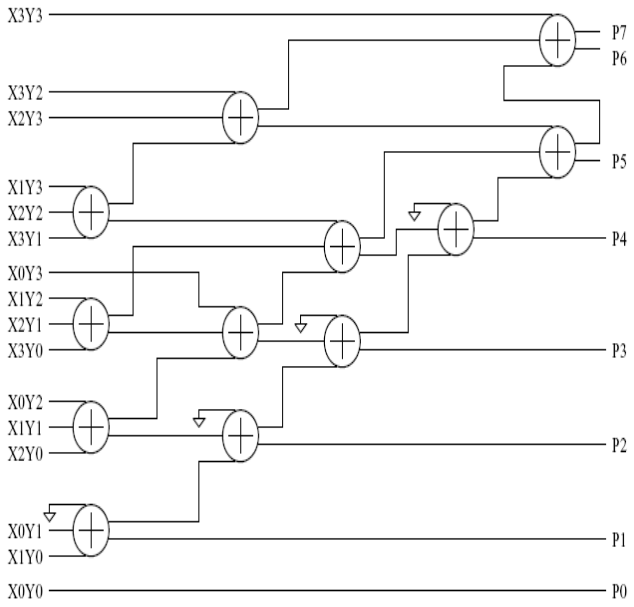

Figure 5: Tree Architecture

5. Simulation Results

The 4-bit multipliers are compared based on the performance parameters like propagation delay, and power dissipation. To achieve better performance, the circuits are designed using CMOS process by MOSIS in 180 nm and 350 technologies at different supply voltages. All the circuits have been designed using TANNER Tool. In this we calculate the Propagation delay and Power dissipation and Transistor count.

5.1 180nm technology at different supply voltages

Table 1: Comparison of Power Dissipation in 4-bit multiplier (array & tree) for various logic designs at different supply voltages in 180nm technology

	CSL	CPL	DPL
ARRAY MULTIPLIER	0.51	0.99	0.49
	0.37	0.67	0.36
	0.28	0.48	0.27
TREE MULTIPLIER	0.52	1.48	0.52
	0.38	1.08	0.39
	0.29	0.74	0.29

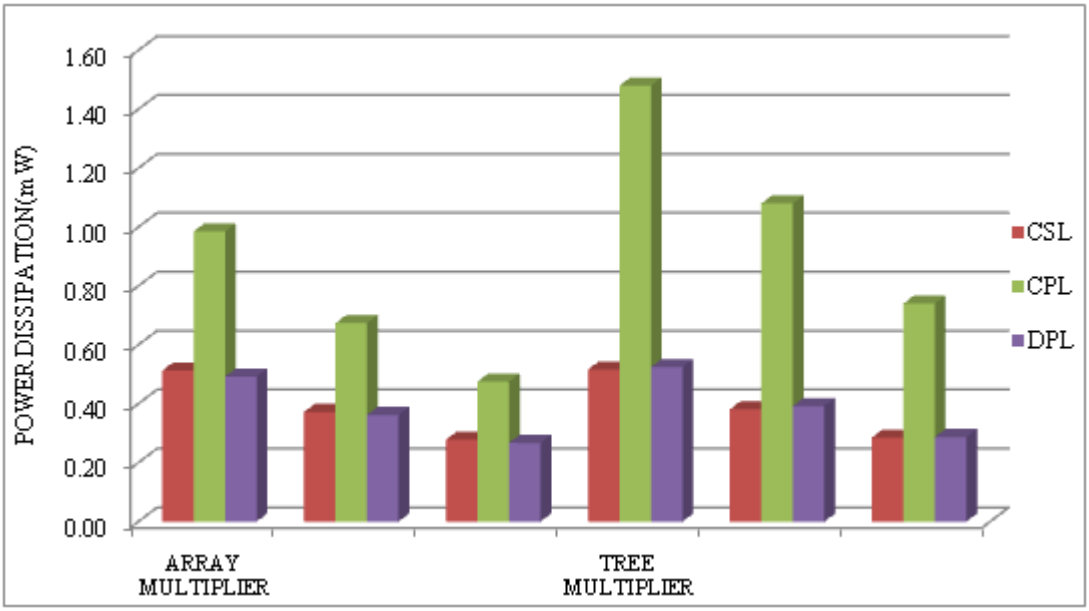

Figure 6: Comparison of Power Dissipation in 4-bit multiplier (array & tree) for various logic designs at different supply voltages in 180nm technology.

Table 2: Comparison of Propagation delay in 4-bit multiplier (array & tree) for various logic designs at different supply voltages in 180nm technology.

	CSL	CPL	DPL
Array Multiplier	0.366	0.373	0.262
	0.391	0.457	0.310
	0.428	0.622	0.357
Tree Multiplier	0.337	0.328	0.270
	0.357	0.447	0.311
	0.409	0.611	0.357

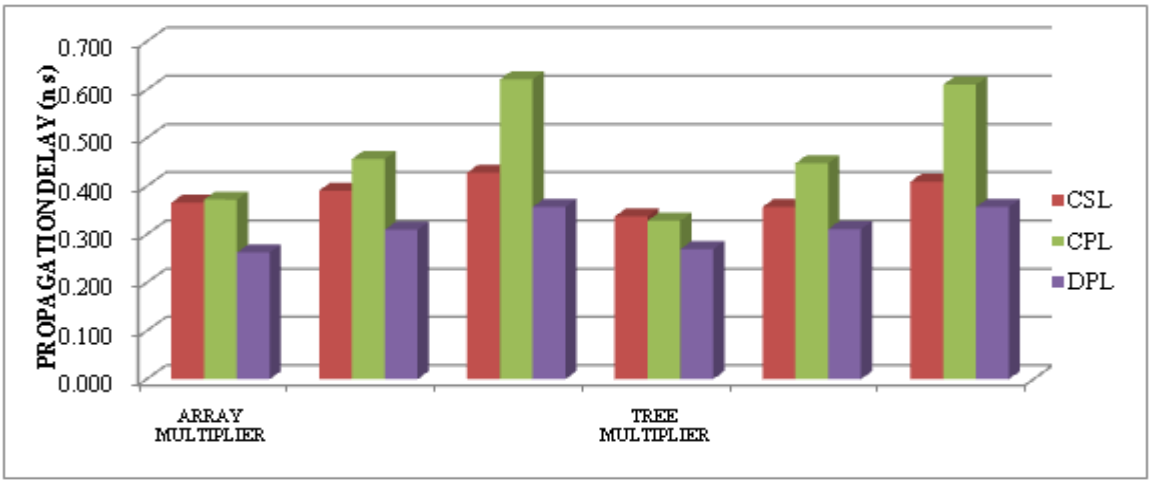

Figure 7: Comparison of Propagation delay in 4-bit multiplier (array & tree) for various logic designs at different supply voltages

Table 3: Comparison of transistor count in 4-bit multiplier (array & tree) for various logic designs at different supply voltages in 180nm technology.

	CSL	CPL	DPL
Array Multiplier	432	384	528
	432	384	528
	432	384	528
Tree Multiplier	432	388	528
	432	388	528
	432	388	528

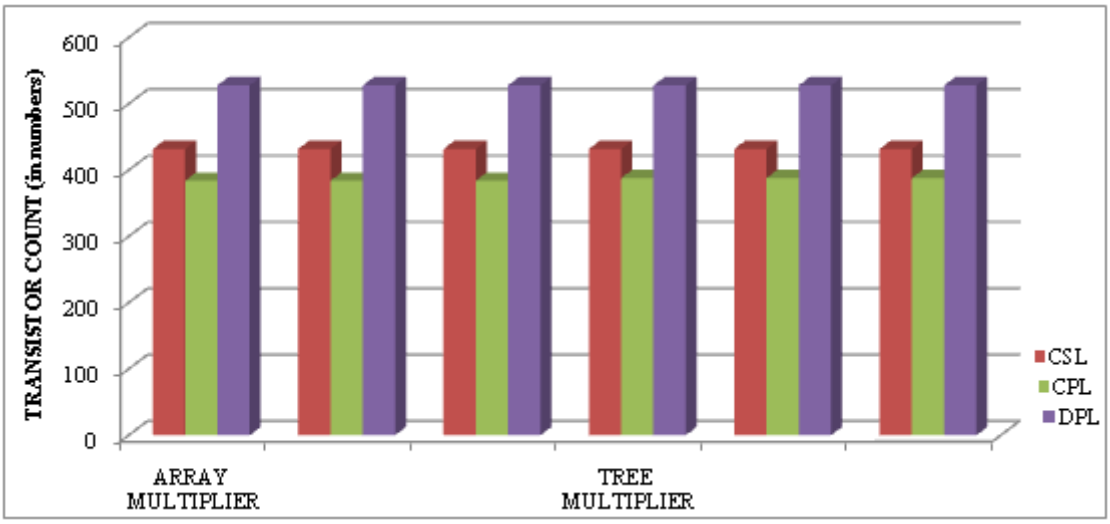

Figure 8: Comparison of transistor count in 4-bit multiplier (array & tree) for various logic designs at different supply voltages

Table 4: Power delay product (m-nj) comparison for different styles at 180nm technology

	CSL	CPL	DPL
ARRAY MULTIPLIER	0.19	0.37	0.13
	0.15	0.31	0.11
	0.12	0.30	0.10
TREE MULTIPLIER	0.17	0.49	0.14
	0.14	0.48	0.12
	0.12	0.45	0.10

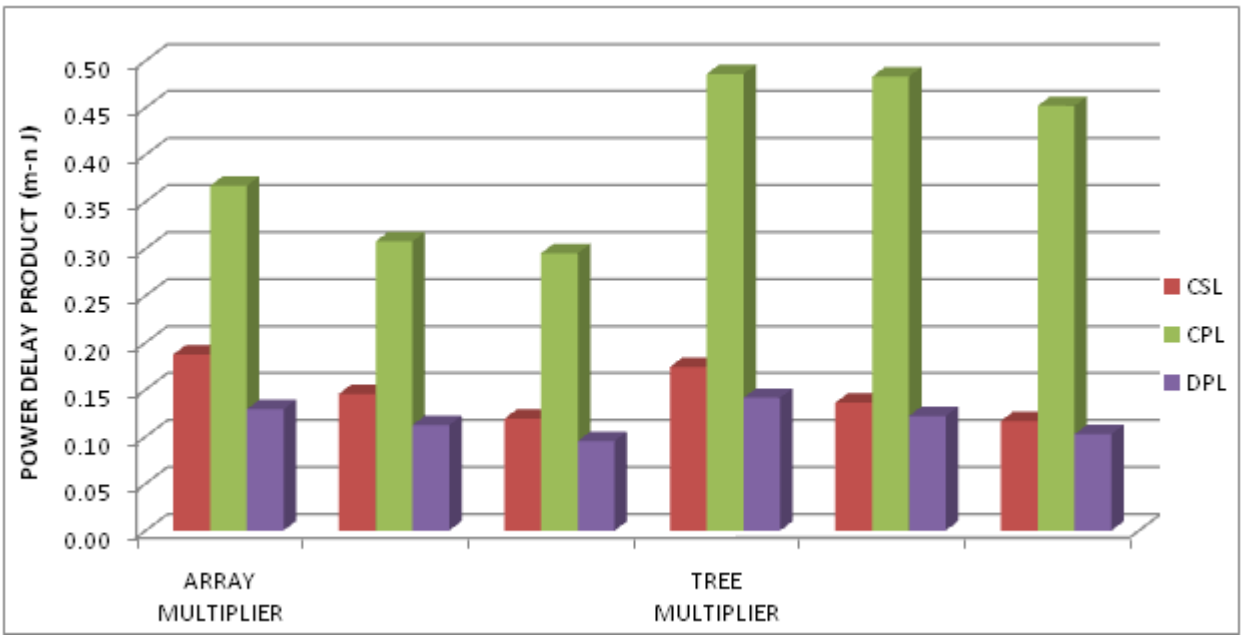

Figure 9: Power delay product (m-nj) comparison for different styles at 180nm

5.2 350nm technology at different supply voltages

Table 5: Comparison of Power Dissipation in 4-bit multiplier (array & tree) for various logic designs at different supply voltages in 350nm technology.

	CSL	CPL	DPL
ARRAY MULTIPLIER	2.87	16.64	12.38
	2.72	3.94	3.94
	2.51	3.46	3.46
TREE MULTIPLIER	2.86	19.60	19.60
	2.69	6.93	6.93
	2.49	6.42	6.42

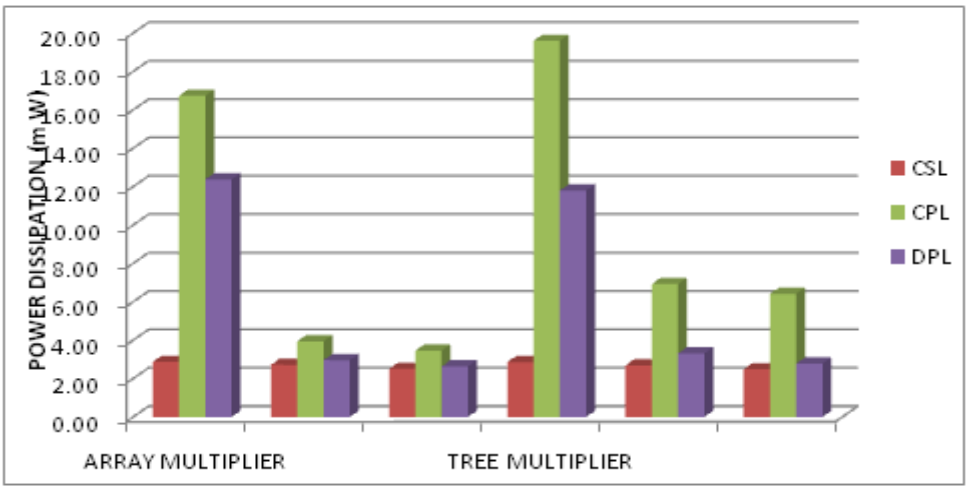

Figure 10: Comparison of Power Dissipation in 4-bit multiplier (array & tree) for various logic designs at different supply voltages

Table 6: Comparison of Propagation delay in 4-bit multiplier (array & tree) for various logic designs at different supply voltages in 350nm technology.

	CSL	*CPL*	*DPL*
ARRAY MULTIPLIER	0.675	0.607	0.530
	0.691	0.634	0.542
	0.943	0.639	0.570
TREE MULTIPLIER	0.605	0.707	0.525
	0.671	0.712	0.545
	0.688	0.765	0.550

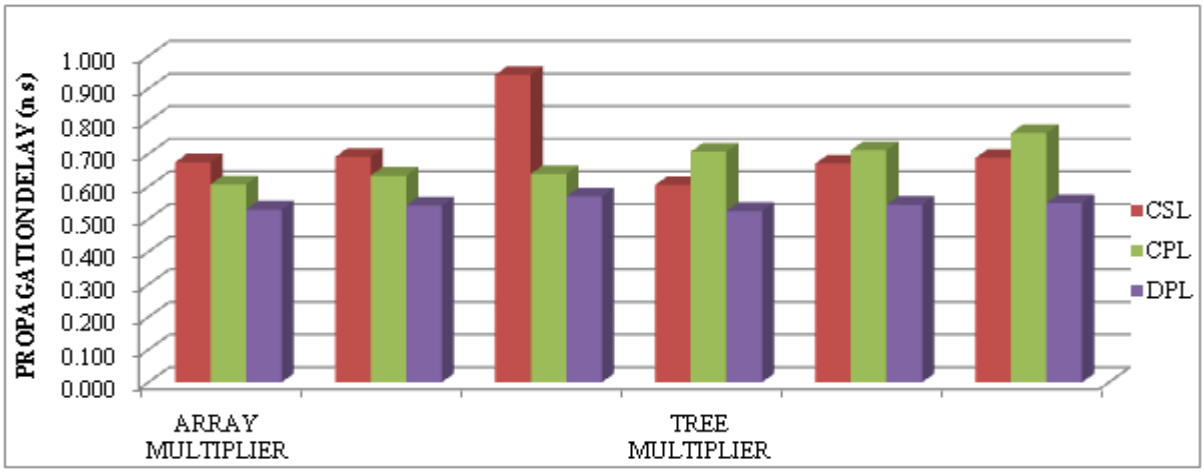

Figure 11: Comparison of Propagation delay in 4-bit multiplier (array & tree) for various logic designs at different supply voltages

Table 7: Comparison of transistor count in 4-bit multiplier (array & tree) for various logic designs at different supply voltages in 350nm technology.

	CSL	*CPL*	*DPL*
ARRAY MULTIPLIER	1.94	10.16	6.56
	1.88	2.50	1.60
	2.37	2.21	1.50
TREE MULTIPLIER	1.73	13.86	6.20
	.180	4.91	1.80
	1.71	4.93	1.53

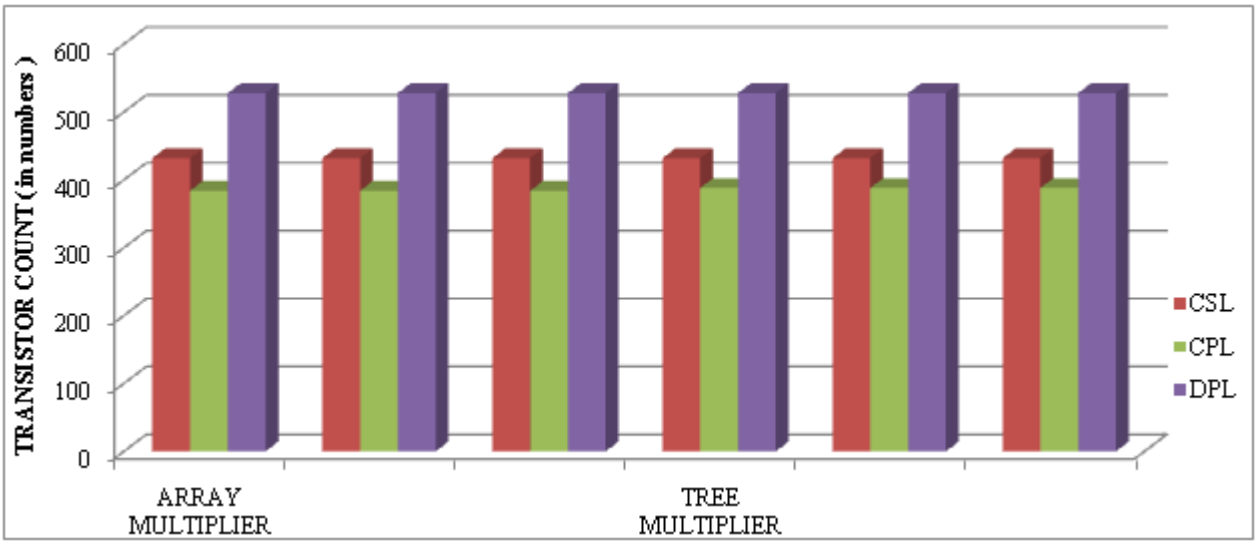

Figure 12: Comparison of transistor count in 4-bit multiplier (array & tree) for various logic designs at different supply voltages in 350nm technology.

Table 8: Power delay product (m-nj) comparison for different styles at 350nm

	CSL	CPL	DPL
Array Multiplier	432	384	528
	432	384	528
	432	384	528
Tree Multiplier	432	388	528
	432	388	528
	432	388	528

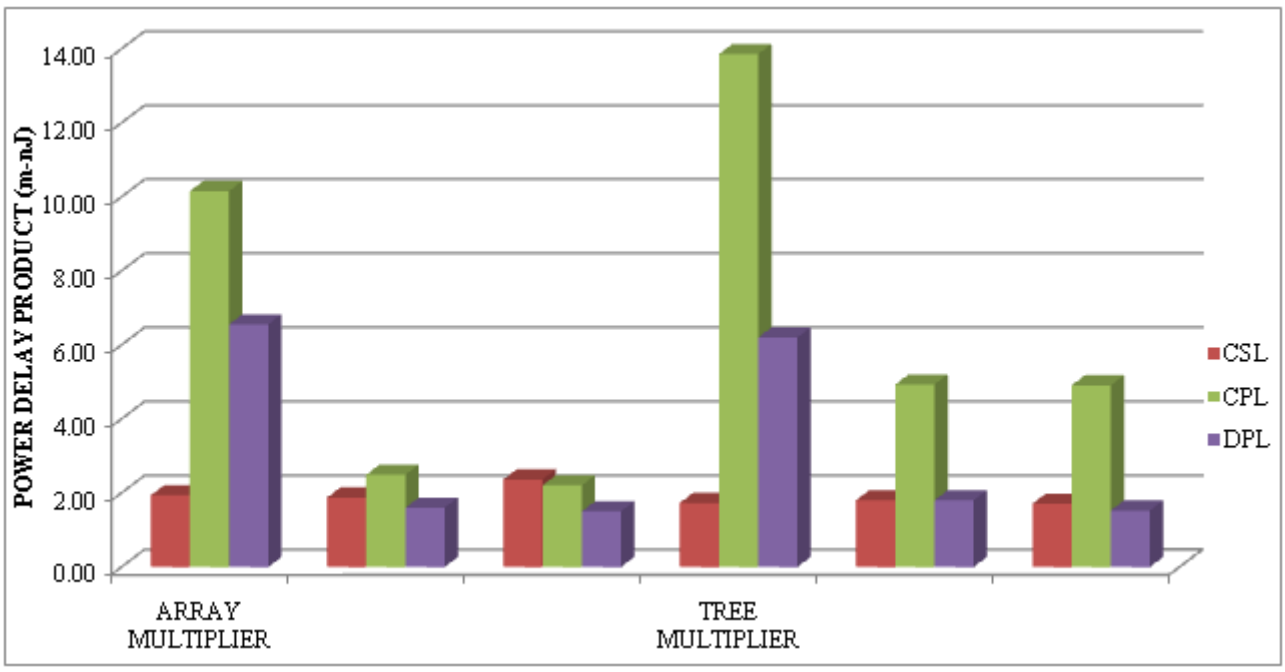

Figure 13: Power delay product (m-nj) comparison for different styles at 350nm

6. Conclusions

It is concluded from Power dissipation comparison that CSL has lowest power dissipation. DPL design style has higher power dissipation but very close to CSL. So it is better to design a system with CSL where low power dissipation is required like portable digital systems e.g. laptop. CPL logic style power dissipation is highest among all. From Propagation delay comparison that DPL design style has least propagation delay time than CSL and CPL. so it is better to use DPL logic style to design a system where fast speed is required. The CSL technique is slowest among all. It is concluded from number of transistors comparison that CPL technique requires less number of transistor to design a system than other two design styles. So electronics circuits designed using CPL logic style will occupy less space on the chip. DPL style has the lowest power- delay product than other two design styles. Thus DPL has the best performance in terms of speed and power dissipation at lower supply voltages. Overall comparison shows that Tree Multipliers are fast or have less propagation delay but consumes more power than Array Multiplier. Also as supply voltage is decreased, the power dissipation decreases and propagation delay increases.

7. Future Scope

Future work in this thesis may include a further scaling down of the technology. Hybrid architecture which is a mixture of Array & Tree architecture can be advised for the proposed multiplier so that speed can be increased and power dissipation can be decreased. To maximize the performance of multiplier 5 to 2 carry save adders can be used to sum the partial products as they are generated.

8. Acknowledgement

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