International Journal of Science and Research (IJSR) ISSN (Online): 2319-7064 Impact Factor (2012): 3.358

Basic study of Junction Field Effect Transistor (JFET)

Kirti

Department of Electronics and Communication Engineering, Haryana, India

Abstract: Junction gate field-effect transistor (JFET) is the simplest type of <u>field-effect transistor</u>. This is three-terminal <u>semiconductor</u> device that can be <u>electronically</u> used as controlled <u>switches</u>, amplifiers, or voltage-controlled <u>resistors</u>. PN junction diode has properties that it injects minority carriers with forward bias and variation of depletion width with reverse bias. These properties play important role in working of the device. FET is a majority carrier device and called unipolar transistor. It is voltage controlled current device having extremely high input impedence.

Keywords: Transistor, PN junction, Biasing, Depletion, Terminal

1. Introduction

JFET is exclusively voltage-controlled device in which there is no need for biasing current. Electric charge flows through a semiconducting channel between source and drain terminals. By applying a reverse bias voltage to a gate terminal, the channel is "pinched off, so that the electric current is impeded or switched off completely. A JFET is usually on when there is no potential difference between its gate and source terminals. If a potential difference of the proper polarity is applied between its gate and source terminals, the JFET will become more resistive to current flow, which means that less current will flow in the channel between the source and drain terminals. Thus, JFETs are sometimes referred to as depletion-mode devices. JFETs can have n-type or p-type channel. In the n-type, if the voltage applied to the gate is less than that applied to the source, the current will be reduced. A JFET has a large input impedance (order of 10^{10} ohms), which means that it has a negligible effect on external components or circuits connected to its gate.



1.1 Construction

Theoretically the construction of JFET is quite simple, but in reality it is very difficult, requiring very pure materials and clean room techniques. JFET is made in different forms, some being made as discrete or single components and others, using planar technology as integrated circuits.

• JFET Diffusion construction: It is the simplest form of construction for a Junction FET (JFET) using diffusion techniques. It uses a small slab of N type semiconductor

into which are infused two P type areas to form the Gate. Current (electrons) flows through the device from source to drain along the N type silicon channel. As only one type of charge carrier (electrons) carry current in N channel JFETs, these transistors are also called "Unipolar" devices.

• JFET planar construction: in this technology the load current flows through the device from source to drain along a channel made of N type silicon. In the planar device the second part of the gate is formed by the P type substrate. P channel JFETs are also available and the principle of operation is the same as the N channel type described here, but polarities of the voltages are of course reversed, and the charge carriers are holes.



Figure 2: Construction model of JFET





JFET-N-Channel and P-channel Schematic Symbol

Volume 3 Issue 9, September 2014 <u>www.ijsr.net</u> Licensed Under Creative Commons Attribution CC BY

1.3 Polarity convention:



1.4 JFET working

JFET operation is just like that of a garden hose. The flow of water through a hose can be controlled by squeezing it to reduce the cross section, similarly the flow of electric charge through a JFET is controlled by constricting the currentcarrying channel. The current also depends on the electric field between source and drain.



Construction of the conducting channel is accomplished using the field effect: a voltage between the gate and source is applied to reverse bias the gate-source pn-junction, thereby widening the depletion layer of this junction encroaching upon the conducting channel and restricting its cross-sectional area. The depletion layer is so-called because it is depleted of mobile carriers and so is electrically nonconducting for practical purposes.^[1]



Figure 4: JFET with no bias voltage

When the depletion layer expands the width of the conduction channel, "pinch-off" is achieved and drain to

source conduction stops. Pinch-off occurs at a particular reverse bias (V_{GS}) of the gate-source junction. The pinch-off voltage (V_p) varies considerably, even among devices of the same typeTo switch off an n-channel device requires a negative gate-source voltage (V_{GS}). Conversely, to switch off a p-channel device requires positive V_{GS} .

In normal operation, the electric field developed by the gate blocks source-drain conduction to some extent. Some JFET devices are symmetrical with respect to the source and drain.



Figure 5: JFET when channel is pinched- off.

But the channel does not totally pinched off because if channel is totally pinched off then no current flows through the channel and there will be no voltage drop through the channel and diode will not be reverse bias now and it forms a symmetrical shape instead of wedge shape. Therefore a minimum amount of current flows through the junction which is called pinched off current and the region is known as saturation region.

2. Characteristics of JFET

JFET characteristics are shown in the figure:

shorted gate JFET characteristics are shown in the figure.



Figure 6: JFET characteristics with shorted gate.

Initially when drain source voltage Vds is zero, there is no attracting potential at the drain, so no current flows inspite of the fact that channel is fully open. So drain current Id is zero. For small applied voltage Vds, N bar acts as simple semiconductor resistor, and drain current increases linearly with increase in Vds up to the knee point. Region to the left of the curve is called channel ohmic region because in this region the JFET behaves as an ordinary resistor.

International Journal of Science and Research (IJSR) ISSN (Online): 2319-7064 Impact Factor (2012): 3.358

With increase in drain current ohmic voltage drop between source and channel region reverse the gate junction. But this biasing is not uniform throughout. Reverse bias more at drain end than that the source end.

Eventually a voltage Vds is reached at which the channel is pinched off. Drain current Id no longer increases with increase in Vds. It gain a constant saturation value. And the voltage ia known as pinch off voltage (Vp) here. And this region is called pinch- off region and sometimes called saturation region. In this region JFET operates as constant Current device. If drain source voltage is increased further, a stage comes where gate- channel junction breaks down. In this region drain current increases rapidly and JFET may get destroyed. And region is known as breakdown region.

It is very interesting to observe that JFET behaves as ordinary register in ohmic region, constant current source in pinch- off region and behaves as constant voltage source in breakdown region.

Lircuit Diagram For Determining Drain Characteristic With External Bias For An N-Channel JFET

3. Drain characteristics with external bias

Figure 7: JFET with external bias.

Above shown characteristics are the characteristics with external biasing.

4. Conclusion

JFET is a field effect transistor which is a voltage controlled current source having extremely high input impedance unlike BJT it is a unipolar junction transistor which is used in many electronic devices as an amplifier.

5. Future Scope

JFET is most popular device in today's electronic world and it will be used for amplifing device and voltage variable registor in future and in many applications in future.

References

- [1] For a discussion of JFET structure and operation, see for example D. Chattopadhyay (2006). "§13.2 Junction fieldeffect transistor (JFET)". *Electronics (fundamentals and applications)*. New Age International. pp. 269 *ff*. ISBN 8122417809.
- [2] J201 data sheet

- [3] Balbir Kumar and Shail B. Jain (2013). *Electronic Devices and Circuits*. PHI Learning Pvt. Ltd. pp. 342–345. ISBN 9788120348448.
- [4] J.b. gupta analog electronics.

Author Profile



Kirti has done **B.Tech** from Matu Ram Institute of Engineering and Management (MRIEM), Rohtak, (Haryana). She is pursuing M.Tech from MERI College of Engineering and Technology, Sampla, Bhadurgarh, Haryana, India