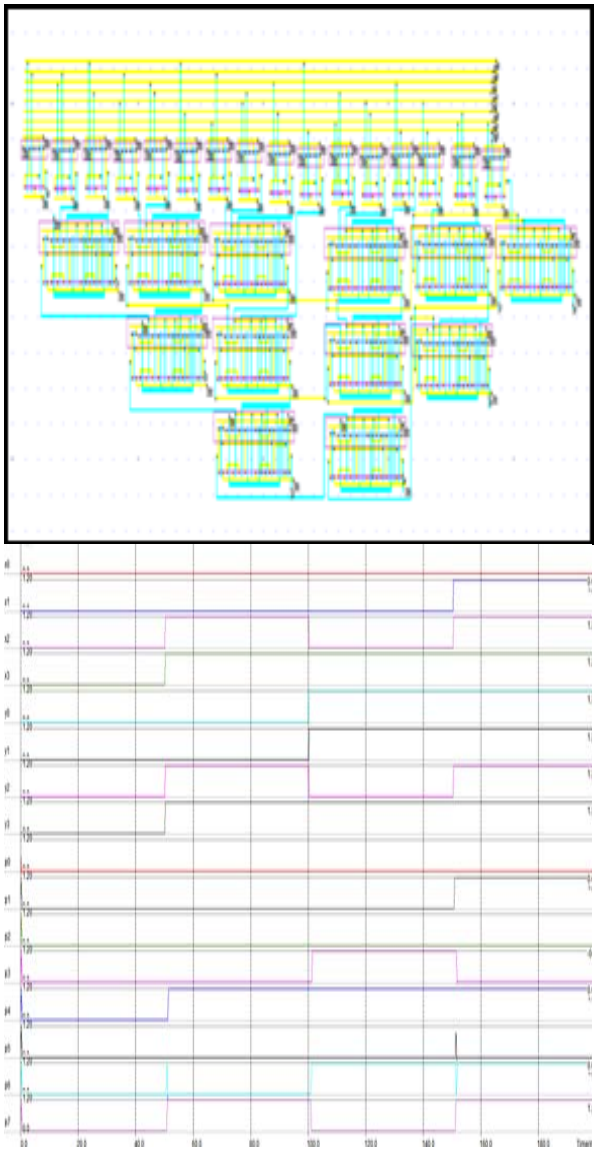

Figure 5.10: Layout of Tree Multiplier and its post layout waveform

4. Power & Delay Analysis

Table II shows the comparison results for Tree Multiplier using different logic styles at 90 nm technology and supply voltage of 2.5v. The table shows the average power consumed, the propagation delay and overall PDP of Tree Multiplier in different logic styles. The results are obtained with load capacitance of 100fF. The maximum power is consumed by CPL Tree Multiplier and minimum power is consumed by CMOS Tree Multiplier. Whereas minimum delay is obtained for DPL Tree Multiplier and maximum delay for CPL Tree Multiplier.

Table 2: 1-bit Comparison of Tree Multiplier using different circuit techniques

Logic Style	*Power Consumed(in µw)*	*Propagation Delay(in ps)*	*PDP ($x10^{-15}$watt sec)*	*Transistor Count*
CMOS	109.137	596.0548	65.051	432
CPL	202.813	623.7514	126.504	464
DPL	149.880	541.6173	81.177	608

5. Conclusion & Future Scope

The overall performance of the Tree Multiplier is compared on the basis of average power consumed , propagation delay, PDP and number of transistors using CMOS logic, CPL logic and DPL logic . Tree Multiplier uses AND gates and Full Adders as its subcomponents. For Tree Multiplier, the DPL logic uses maximum number of transistors and CMOS uses minimum number of transistors. The minimum power is consumed by CMOS logic and minimum propagation delay is found out for DPL logic. CMOS logic has the minimum PDP value. As it can be concluded from above discussion that minimum delay is exhibited by DPL logic but with maximum number of transistor count. The CMOS logic provides the best PDP for Tree Multiplier with minimum power consumption. As Tree multiplier is a fast multiplier used for large operands, high order tree multiplier can be implemented using other methods for different performance parameters and also layouts of Tree Multiplier architectures for CPL and DPL logic can be designed.

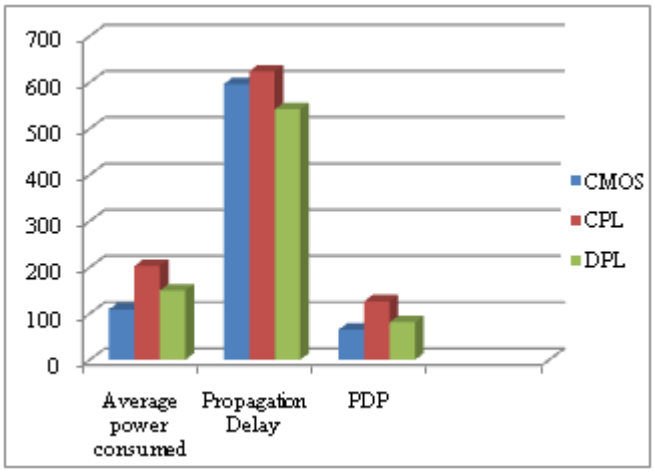

Figure 14: comparison of the Tree multiplier using different logic styles

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