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Low Power, Low Voltage 95.1-dB Linear Variable Gain Amplifier with Diode Connected Load

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Abstract: ***A less gain error CMOS variable gain amplifier (VGA) with addition of diode connected load is presented. No additional circuit for gain control is required in the proposed design used in a Automatic gain control (AGC). A high linearity performance and a wide gain control voltage from 0.68 to 1V are achieved. Proposed VGA is fabricated in a 45nm CMOS technology and shows a gain range 104.64dB (-64.54dB to 40.10dB) and linear range 95.1dB (at frequency 67.78 KHz to 58.53MHz) with a linearity error 0.077 dB. The gain bandwidth is over 58.53 MHz at all gain settings. The whole circuit, occupying less area with 0.6uA current consumption and 0.6uW power consumption at 1V supply.***

Keywords: dB linear, variable gain amplifier (VGA), diode connected load, automatic gain control.

1. Introduction

The variable gain amplifier (VGA) is an indispensable building block to maximize the dynamic range of modern wireless communication systems [1]–[3], as well as medical equipment, hearing aids, disk drives, and so on [4]–[7]. A VGA is typically employed in a feedback loop to realize automatic gain control (AGC). The VGA of an AGC loop is used to control the transmission signal power or to adjust the received signal amplitude. There are two possible approaches to build the VGA. One is to build a discrete gain step VGA with a digital control signal [8]–[10], and the other is to build a continuous VGA controlled by an analog gain control signal [1]–[7].

In general, digitally controlled VGAs use binary weighted arrays of resistors or capacitors for gain variations [11] and analog VGAs adopt a Variable transconductance or a variable resistance to control the gain. For a code division multiple access (CDMA) system requiring a power control range larger than 80 dB, the VGA with continuously variable gains is preferred because it avoids signal phase discontinuity that is expected to cause problems [3], [12] and it reduces the large number of control bits required with digitally controlled VGAs. Until now, VGA circuits based on various technologies such as bipolar, BiCMOS, and CMOS have been introduced [1]–[12].

Recently however, CMOS VGAs are preferred due to the low cost and easy integration with other CMOS analog/digital parts. An important requirement for a CMOS VGA is a decibel-linear gain control characteristic, where the gain of the VGA changes exponentially with the control signal. The exponential gain control is required to achieve a wide dynamic range and to maintain the AGC loop settling time independent of the input signal level [12],[13]. However, it is difficult to realize this exponential function due to its inherent square or linear characteristics in CMOS technology. Although a transistor operating in a subthreshold region has an exponential characteristic, it is generally not preferred due to other unfavorable effects such as noise and bandwidth [14].

Another possible method is to use parasitic bipolar transistors to generate the desired exponential function. The linear-in-decibel gain control signal is generated using the relationship between a collector current (I_C) and base-to-emitter voltage (V_{BE}). This is strongly dependent on the temperature and processes. Therefore, various compensation techniques that guard against the temperature and the process variations are required to have an accurate signal power control mechanism. Obviously, temperature compensation is needed to control the output level in a linear-in-decibel manner over a wide dynamic range [15].

It is also preferable to minimize the resolution of the digital-to-analog converter, which drives the gain control terminal [12]. The method used to generate the temperature-independent exponential function requires complex circuits However; this method achieves a linear-in-decibel controlled range of more than 30 dB per stage, which is difficult to achieve using a pseudo exponential function in a short-channel CMOS. Another important aspect of a wideband VGA is a large bandwidth. There are many systems for high-speed data communications such as ultra-wideband (UWB) systems, wireless local area networks (LANs), and Bluetooth [16], [17]. These systems provide a high data rate with relatively low power consumption in short-range wireless communications. For high-speed data communication, the bandwidth of a VGA must be very wide. Therefore, a wideband VGA is a key component.

In a wireless receiver, variable gain amplifiers (VGA) are usually employed in an automatic gain control (AGC) loop, to provide an optimum input power to the baseband analog-to- digital converters (ADC) for unpredictable received signal strength from the antenna, so as to maximize the signal-to-noise ratio (SNR) performance.

While discrete-gain VGAs controlled by digital signals have a disadvantage in complicated additive digital gain control

circuits to achieve an AGC function, continuous-gain VGAs controlled by analog signals are preferred for their simplified gain control circuits. In most AGC loops, an exponential gain control characteristic of the VGA is required to maintain the settling time of the AGC independent of the input signal level [18]. For this reason, an exponential function in a CMOS implementation is approximated by CMOS transistors in the saturation region with a square-law characteristic [19-21].

In this way, an exponential gain control circuit has to be implemented, which shows sensitivity to process and temperature variations, making this method less robust. Moreover, since an AGC is the last stage of an RFID receiver front-end. [22], the linearity performance of a VGA is critical for the whole system. However, a conventional Gilbert-cell VGA with a gain tuned by steering tail currents has a low linearity. dB- linear VGA with addition of diode connected load is presented in this paper.

Proposed method reduces power consumption and current consumption without use of any additional circuits, resulting in a robust VGA require less area.

2. Proposed Design

In this paper dB- linear VGA with addition of diode connected load is presented. A VGA provides a means of amplifying such signals, with less distortion or saturation, and can be used as the controlled element of an Automatic Gain Control (AGC) circuit in a receiver, or as the controlling amplifier in a Timed-Gain-Control circuit of an Ultrasound system. The load of differential pair need not be implemented by linear resistor so it is desirable to replace resistor with MOS. The main reason in this M3, M4 are always in saturation region.

Because the drain and gate have the same potential MOS is three terminal device which can be used as a resistor (two terminal device) by shorting the gate to the own drain. Resistor takes more area & noisier so that resistor is replaced by mos. the basic differential amplifier with diode connected load is shown in figure 1.

Voltage gain is A_v is given by

$A_v = -g_{mN} (g_{mP}^{-1} || r_{ON} || r_{OP})$

$\approx - (g_{mN}/g_{mP})$

Where subscripts N and P denotes NMOS and PMOS, respectively.

$A_v \approx -\sqrt{[\mu_n (W/L)_N / \mu_p (W/L)_P]}$

μ_n and μ_p are the mobility of NMOS and PMOS respectively.

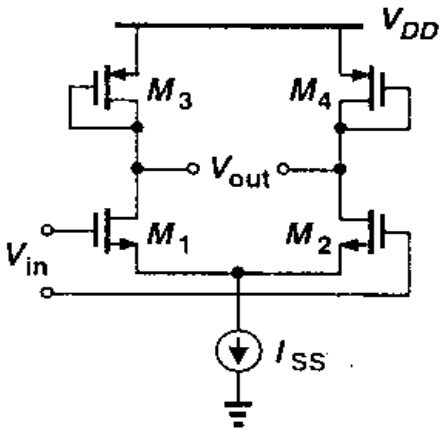

Figure 1: Basic Differential Amplifier with Diode Connected Load

A variable gain amplifier is a special kind of amplifier whose gain can be dynamically controlled in 'real-time' by an externally applied control voltage. In its simplest form, it can be visualized as an amplifier with an electronic gain control. Proposed circuit of VGA is shown in fig. 3. Where N1, N2 is the n-type differential input pairs. Control voltage is applied at the gate of N3 MOS, which controls the gain of device. Three terminals MOS is in saturation region act as amplifier and in linear region act as a resistor.

Become two terminal devices and in saturation region it work as resistor. P1 and P4 are two terminal devices which are connected at load side. Proposed circuit is operated at very less power supply and provides large dB- linear range with less power consumption.

3. Simulation Result

45-nm CMOS technology is used to fabricate proposed VGA. The current consumption of this VGA is 0.6(uA) and do not require extra circuit so area is reduces. Proposed VGA having gain range (-64.54dB to 40.10dB) 104.64dB and gain error 0.077dB at 1v power supply. Proposed VGA can boost dB-linear range with less gain error .Simulation result is shown in table I

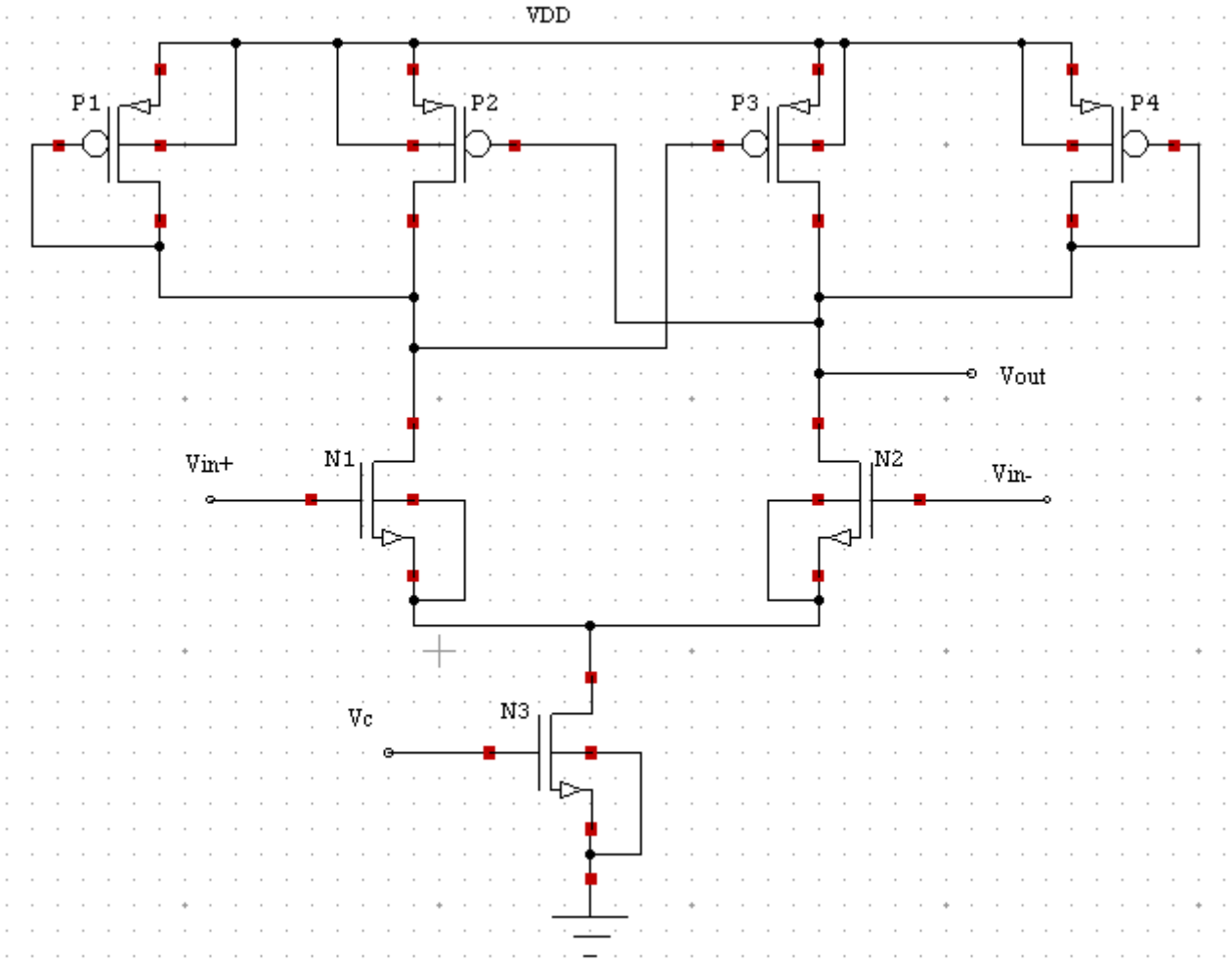

Figure 3: Prorposed Diagram of VGA

The calculation of CMRR (common mode rejection ratio) and PSRR (power supply rejection ratio) is described below-

Calculation of CMRR -

CMRR= (Ad/Ac)
Ad= open loop gain =100.25
Ac= common mode gain =0.486
CMRR (dB) =20log (Ad/Ac)
CMRR=46.28dB

Calculation of PSRR -

PSRR= (Vsupply/Vout) Ad
PSRR (dB) =20log [(Vsupply/Vout) Ad]
PSRR (dB) =48.72

Table 1: Simulation Result Summary

Design	*Result*
technology	45nm
Supply voltage	1v
Power consumption(uW)	0.6
Current consumption(uA)without buffer	0.6
Gain range(dB)	-64.54 to 40.10
Gain error(dB)%	0.077
dB-linear range(dB)	95.1
Slew rate(V/us)	152.50
CMRR(dB)	46.19
PSRR(dB)	48.8
gain bandwidth(MHz)	58.53
UGBW(MHz)	1.45

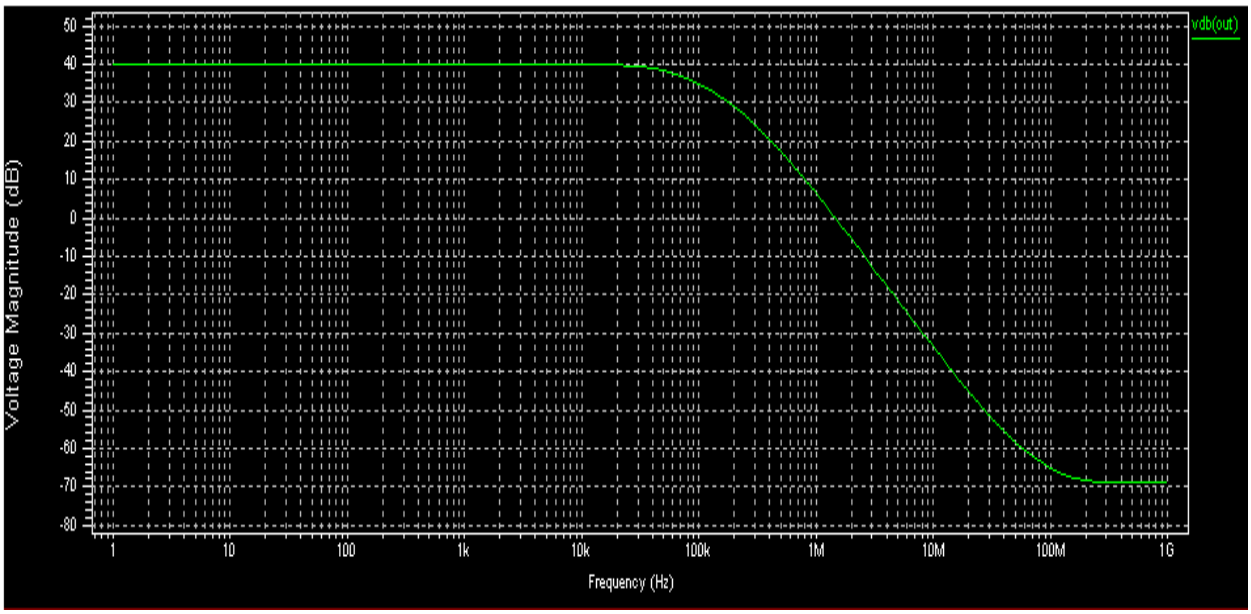

Figure 4: Gain (dB) Versus Frequency (Hz) Graph

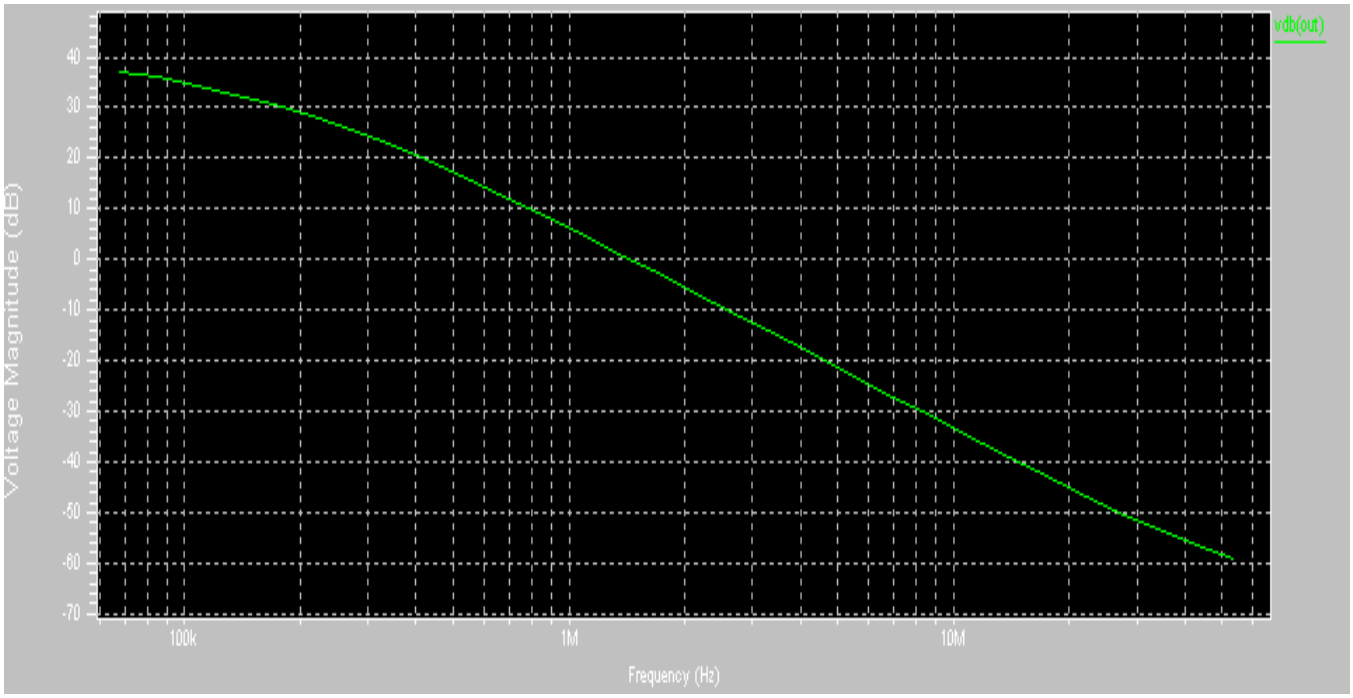

Figure 5: Measured gain of dB –linear VGA at 67.78 KHz to 58.53MHz

4. Conclusion

The circuit performance can be characterized by that fact that no addition gain control circuit is needed and by the high linearity performance. A dB linear VGA with diode connected load has been presented. The VGA has a 104.6dB (-64.54dB to 40.10dB) gain control range. It consumes a total current of 0.6 uA (without buffer) under a single power of 1 V and occupies less area .Proposed VGA is implemented in a 45nm-CMOS technology with 1 V supply voltage with power dissipation of less than 0.6uW.

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