3. Results and Discussion

3.1 IP Integration

The following chapter explains about Vivado software design suite and simulation results of AES. The software implementation is done on the VIVADO Design suit. Firstly Zynq device is configured as per given requirements and a hardware platform of VIVADO tool generates ARM IP cores (PS hardware). The defined IP core is also added to the tool generated hardware to meet the specified requirements. When IP is added then corresponding HDL code is generated automatically. After then required pins of different IPs interconnected and routed to I/Os. The hardware configuration information is exported to the SDK (software development kit).

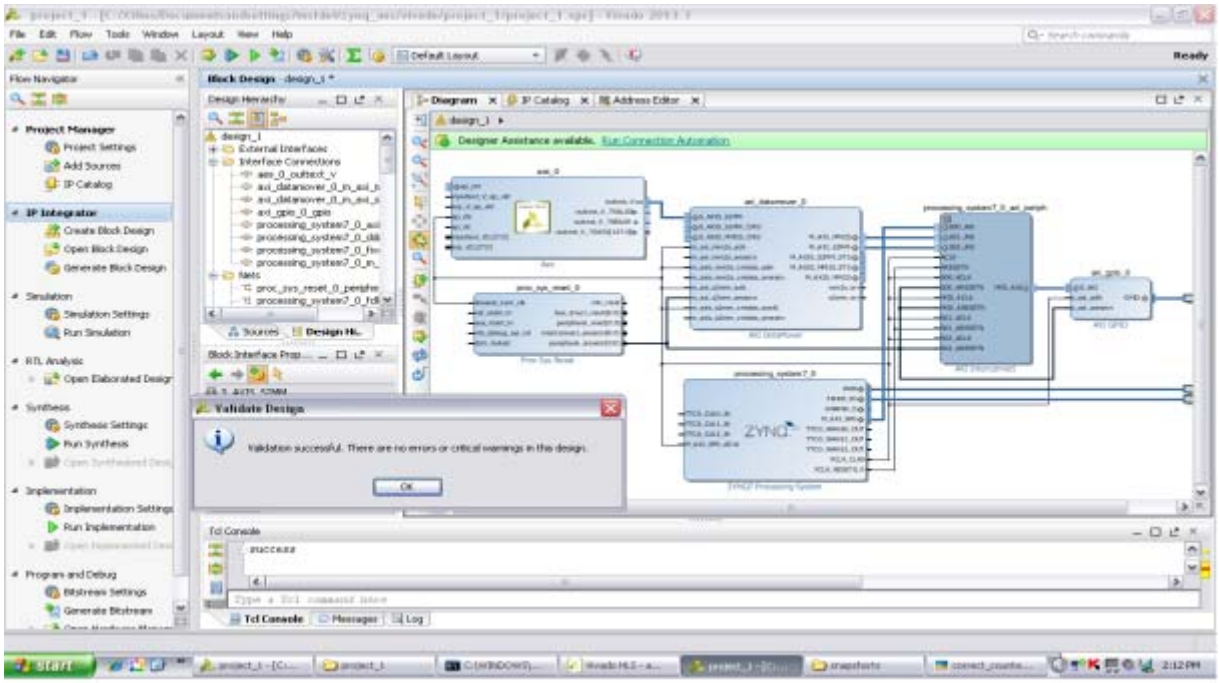

Figure 9: IP Integration

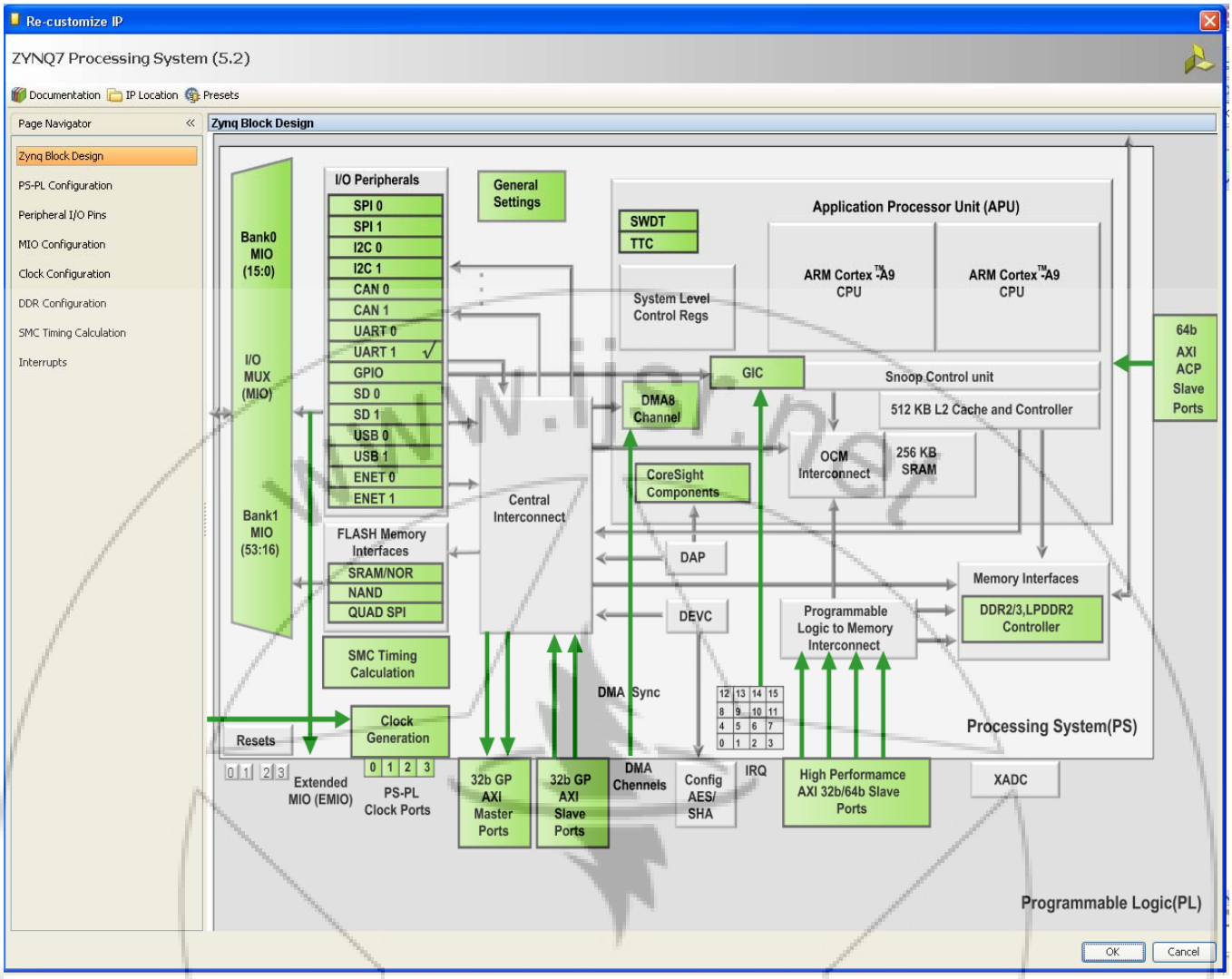

Figure 10: FPGA Interface

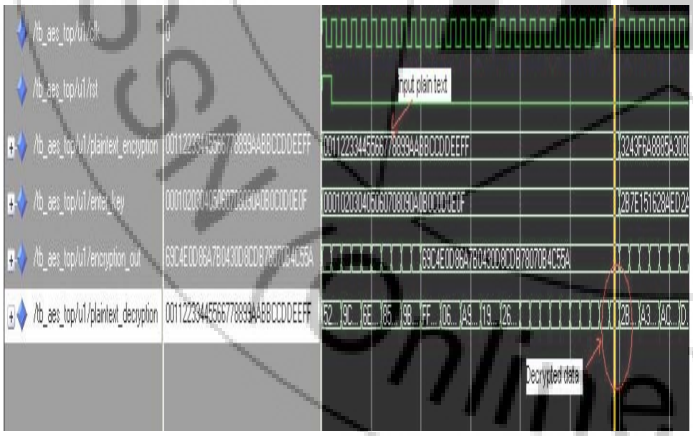

Figure 11: AES Simulation Results

4. Conclusion

Secured data transmission systems on Zynq SoC are presented in this paper. It consists of several different modules. Each of these modules are, implemented and tested on different development platforms. This hardware implementation is relatively simple and easily integrated to any platform due to the independence to Vendor specific macros. The advanced encryption standard (AES) algorithms are used. Thus it achieves high speed at low area cost. Algorithms and implementations are presented in above figures. In present systems Telemetry systems are occupies more space, size and weight. Using zynq Soc it occupies less space and weight.

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