with VHDL coding. The experimental analysis is required for the implementation of technique. There are the VHDL coding used with the Xilinx-13.1 and simulation done with the ISIM simulator.

Synthesis code first written for a Full adder circuit without using VID concept. After synthesize the code simulation done and timing report generated which provides the gate delays in the circuit and also defines the design specification for circuit. The RTL schematic and synthesis report of the circuit without using VID technique given as:

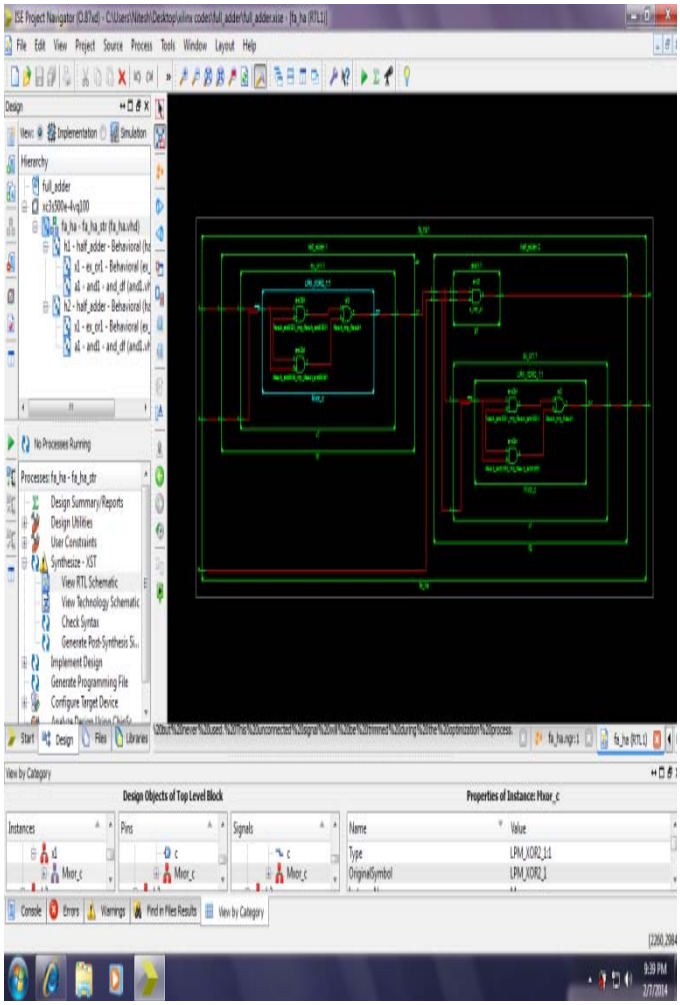

Figure 1: RTL schematic of Full Adder circuit

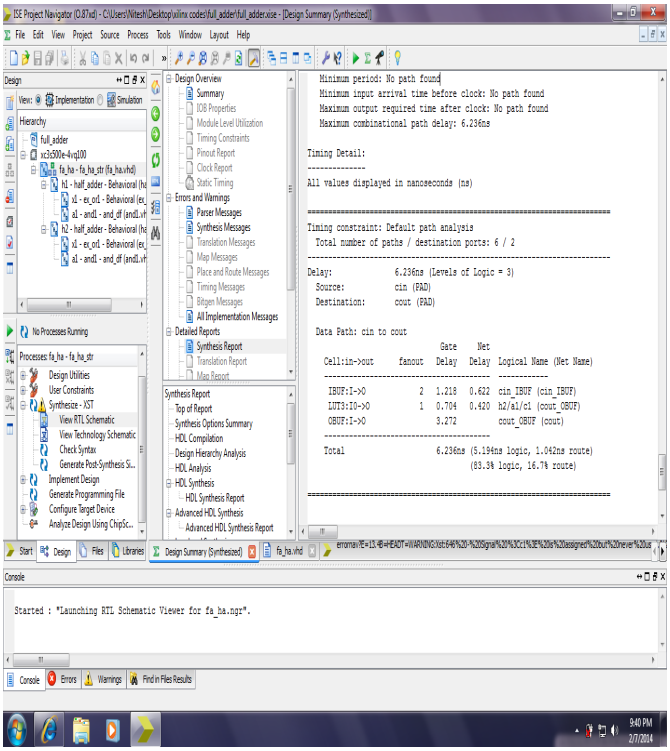

Figure 2: Timing Report of Full Adder

Then again improved the code with VID technique and compare the timing results of both. The power optimization is a main component in low power design with CMOS devices which achieved with the VID technique.

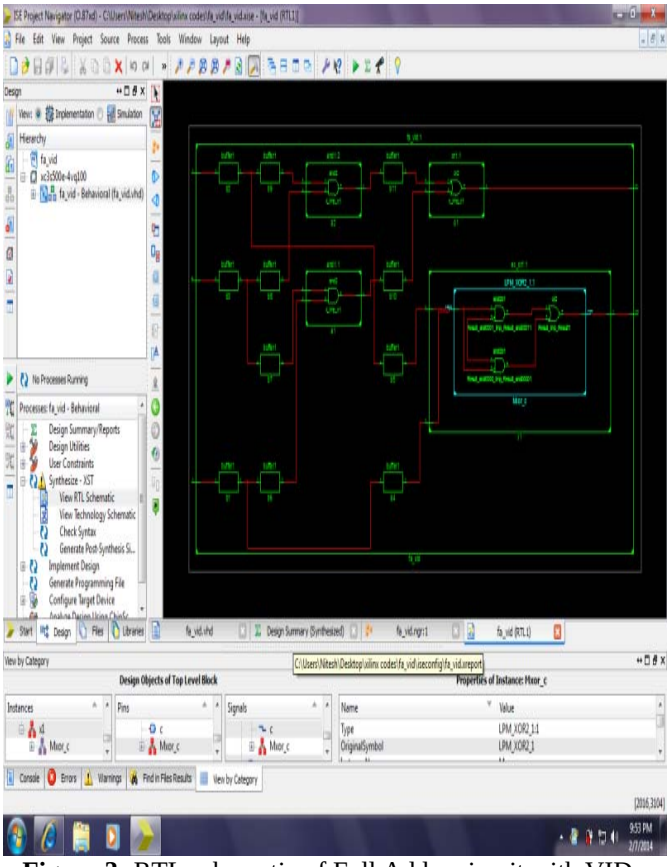

Figure 3: RTL schematic of Full Adder circuit with VID concept

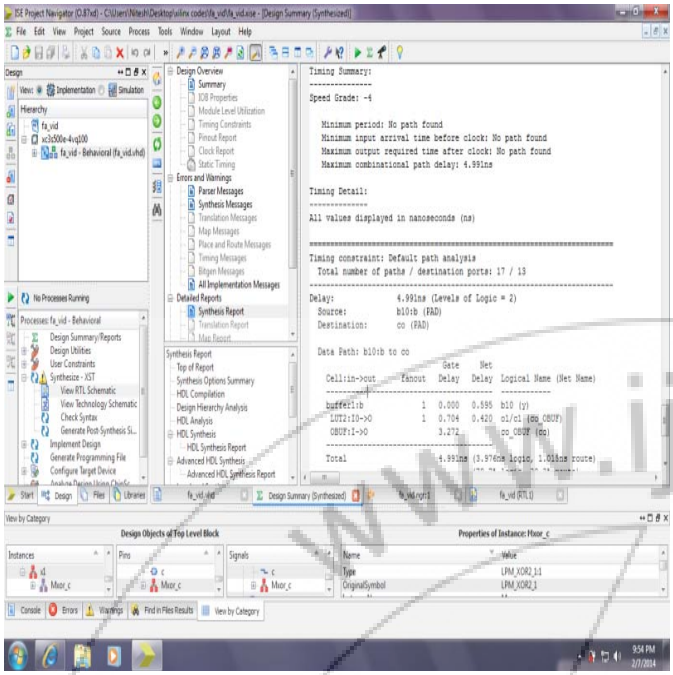

Figure 4: Timing Report of Full Adder using VID concept

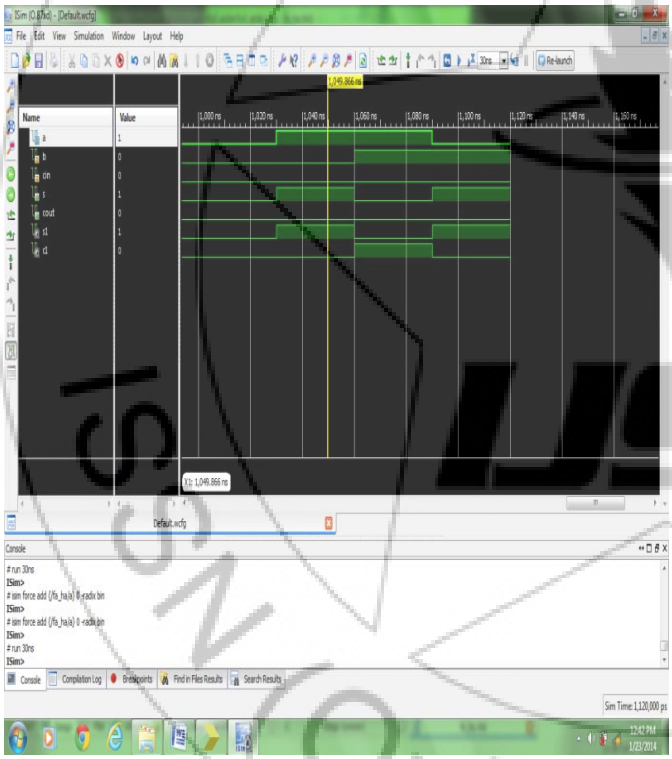

Figure 5: Simulation results of Full Adder circuit

RTL schematic and timing report of both conditions given by figures. After compare the timing report of both conditions we get optimized Full adder circuit with 50% of power.

5. Conclusion

This paper considered the VID technique for reduction of dynamic power in CMOS logic circuits. There is Full adder circuit implemented using VID technique which gives better result. 50% of power optimized in the circuit. This technique used buffer insertion at critical path delays which reduced the delay of these paths. With this technique the area increased due to buffer insertion so technique can be modified with area improvement.

6. Acknowledgment

I would like to express by deep gratitude and thanks to Dr. Mahesh Bundele, Coordinator and Research, in Poornima University and my Guide Mr. Sanjay Sharma, for giving me an opportunity to work under his guidance.

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