Implementation of Quantum dot Cellular Automata based Novel Full Adder and Full Subtractor

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Abstract: *Quantum-dot cellular automaton (QCA) is an up-coming nanotechnology in the area of nanoelectronics and is found to be an alternative solution to replace conventional CMOS technology for several reasons. It has attractive features such as faster speed, smaller size, and low power consumption compared to transistor-based technology. The experiments carried out in QCA demonstrated and realized the fundamental digital blocks. This paper demonstrates designing combinational circuits based on quantum-dot cellular automata (QCA), which covers a way to implement logic and all interconnections with homogeneous layer of cells. The novel implementation of full adder and full subtractor with less area, circuit complexity and clock delays are presented in this paper. Several full adders have been reported in literature but many other QCA based circuit implementations, including full subtractor, have not been reported in open literature. Comparative study illustrates significant improvements in our design as compared to traditional approaches. The correct logical functionalities of presented structures have been authenticated using QCADesigner tool.*

Keywords: QCA, Combinational Circuits, Full Adder, Full Subtractor, QCA Designer

1. Introduction

Quantum–dot Cellular Automata (QCA) is a novel nanotechnology that has attracted a lot of attention over the last two decades. This technology promises extremely low power consumption, high speed and extremely dense structure for implementing any logical circuit. Current CMOS devices are becoming resistant to scaling. The most important reason is the power density. Nanotechnology is a possible alternative to these problems and the ITRS report [1] summarizes several potential solutions. QCA is an interesting option and was introduced in 1993 [2]. QCA creates general computational functionality at the nano scale by simply controlling the position of single electron. Circuits based on the QCA technology solve series of problems which the traditional devices face when it enters the domain of nano meter scale. QCA has gained significant popularity in recent years, which is due to the growing interest in creating computing devices and implementing any logical function in QCA. The basic structure of the QCA cell is a set of four charge containers called quantum dots positioned at the corners of a square as shown in Fig. 1(a) [3-4]. The binary representation of QCA cell can be specified with its polarization. The polarization levels as shown in Fig. 1(b) are P=-1, representing binary '0' and P=+1 representing binary '1' [4]. The basic building block of QCA circuits is majority gate. Hence, there are some differences between this technology and other technologies such as CMOS. To convert QCA to a serious substitute candidate for CMOS, all the researches done on CMOS should be performed on QCA. For QCA circuit elements, basic logic gates are required. Every gate in QCA takes an advantage of geometry of cells. The inverter and a three-input majority gate [5] is shown in Fig. 1(c) and Fig. 1(d).The majority gate can function as an AND and OR gate by setting one input (one of the three inputs of the majority gate) to a fixed polar

cell either P= + 1 which represents logic 1, or P=-1 which represents logic 0. When a single input is set to logic 0, then the output is said to be AND of the other two inputs. Moreover if a single input is set to logic 1, then the output will be OR of the other two inputs. With AND gates, OR gates and inverters, any logical function can be realized. Several examples of optimal gate construction are introduced in [6-9]. Adder and subtractor component is used for the design of many computation systems and functional circuits. Works presented in [10-15] introduced different kinds of half/full adder designs with different number of majority gates and the full adder design proposed in [12] has better performance compared to the other designs. Works presented in [16-21] have implemented five different schemes for XOR and the presented XOR in [20] is better than other designs in terms of complexity, area and delay. XOR is a useful component for the design of many logical and functional circuits. Recently, works present in [22-23] has designed code converters and pseudo-code generators by. XOR gate is a vital component to design adder and Subtractor circuits. The design and implementation of full adder and Subtractor have proposed in this paper with only one homogenous layer of cells.

The paper is organized as follows. In Section II, a brief review of previous full adder and proposed full adder has been discussed. In section III proposed full subtractor has been demonstrated. Comparisons have been provided in section IV. Conclusions are presented in section V. Finally future work is presented in section VI.
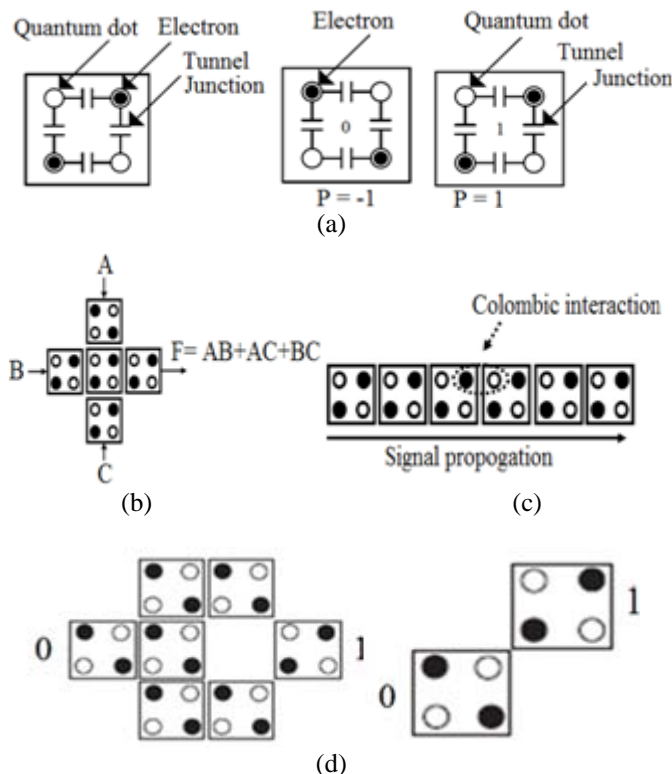
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(a)

(b)   (c)

(d)

Figure 1: (a) QCA cells with four quantum dots in two possible cell polarizations [4] (b) Majority gate [5] (c) QCA binary wire [4] (d) QCA Inverters [4]

2. Proposed QCA Layout of Full Adders

Digital computers perform various arithmetic operations. The most basic operation is the addition. The addition operation is achieved by majority logic that can reduce the overall number of gates required to create the adder circuits. Full adders are the main member of computational systems because adders can implement other operations. The implementation of full adders are presented in [10-15] has been used for comparison. The comparative study of adder circuits, is present in Table 1.

The general logic function of Majority full adder is expressed as:

$$Mv (A' Mv (Mv (B', C, 0), 1), 0), 1) \quad (1)$$

Sum can be represented in Majority logic as:

$$Sum = Mv [C'out, Cin, Mv (A, B, C' in)]$$

Carry Cout can be represented in Majority logic as:

$$Cout = Mv (A, B, Cin)$$

The QCA layout of proposed full adder is shown in Fig. 2(a). The design is simple using homogeneous layer of 90^0 cells. The simulation results of proposed design is shown in Fig. 2(b). It is inferable from simulation results that the proposed adder design consumes smaller area, has less latency and also has less complexity compared to the previous designs [10-15]. The proposed adder design consumes smaller area of 0.12 um^2, with less complexity of 108 cells. The simulation result demonstrated that the proposed design requires 2.5 clock cycles.
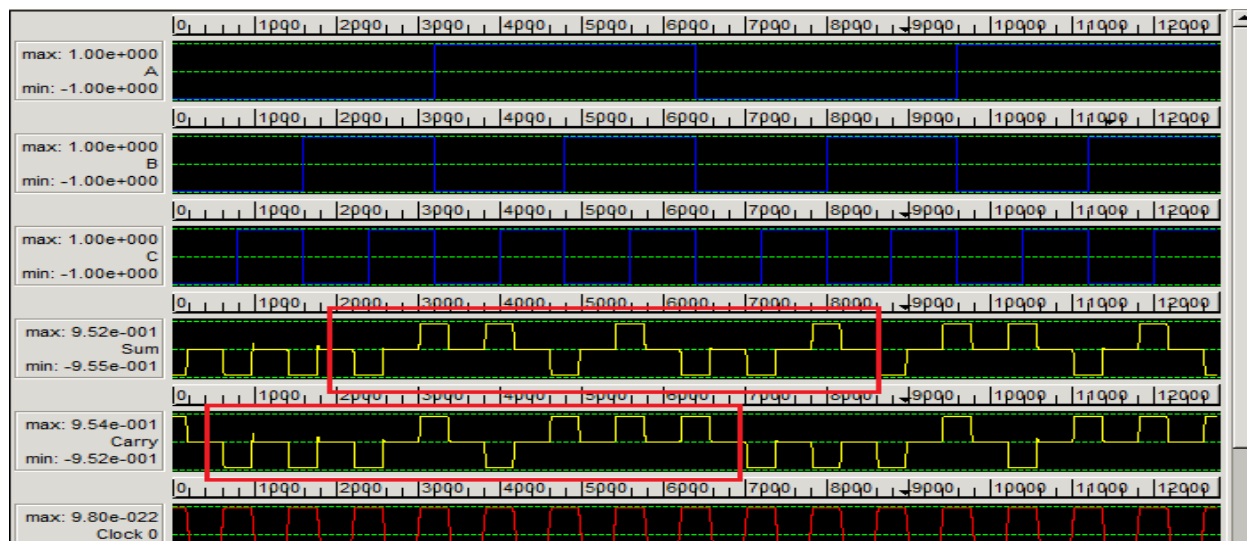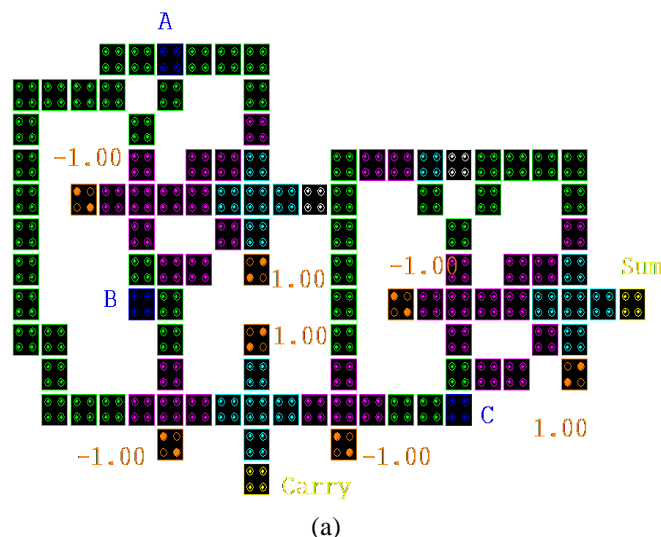

(a)

(b)

Figure 2: (a) The layout of proposed adder design (b) Simulation result

3. Proposed QCA Layout of Full Subtractor

As like full adder, full subtractor is the main member of computational systems and can perform various airthmatic operations. A full subtractor is a combinational circuit that performs a subtraction between two bits, taking into account that a 1 may have been borrowed by a lower significant bit.

The general logic function of Majority full subtractor is expressed as:
 MV (A' MV (MV (B', C, 0), 1), 0), 1) (2)
Difference can be represented in Majority logic as:
    Difference = MV [C 'out, Cin, MV (A, B, C ' in)]
Borrow can be represented in Majority logic as:
 Borrow = MV (A, B', Cin)
The QCA implementation of full subtractor has not been reported in open literature. The layout of proposed full subtractor is shown in Fig. 3(a). The design doesnot use any crossovers and consists of homogeneous layer of 90^0 cells. The simulation results of proposed design is shown in Fig. 3(b). The proposed subtractor consumes smaller area of 0.12 um^2, with circuit complexity of 107 cells. The simulation

signifies that the proposed subtractor requires 2.5 clock cycles.
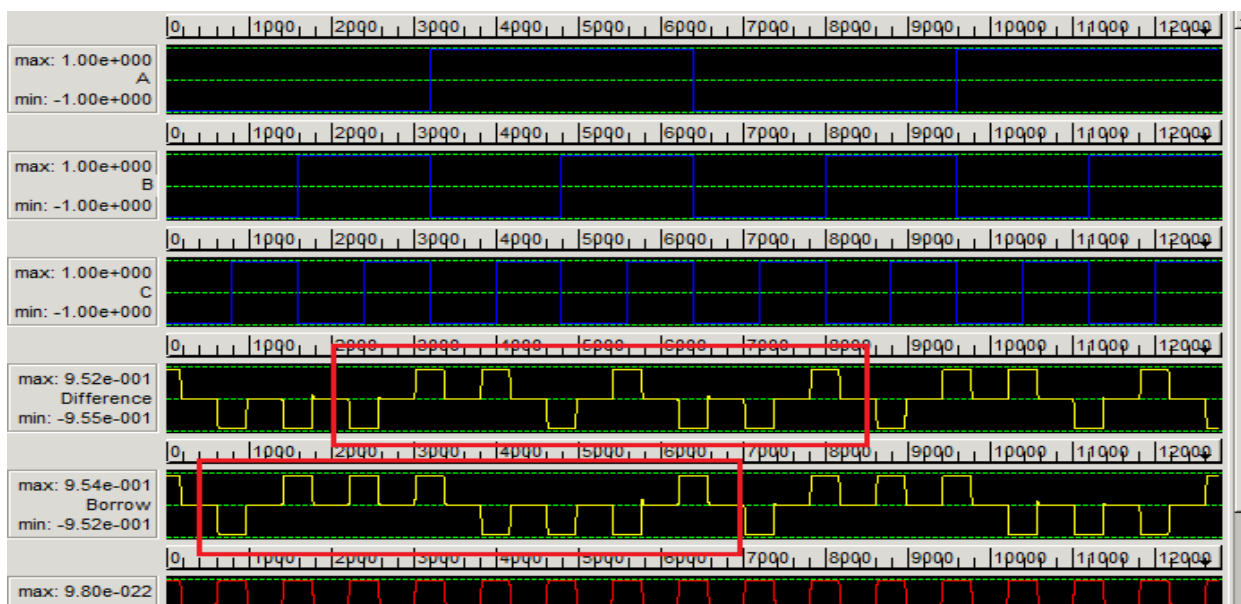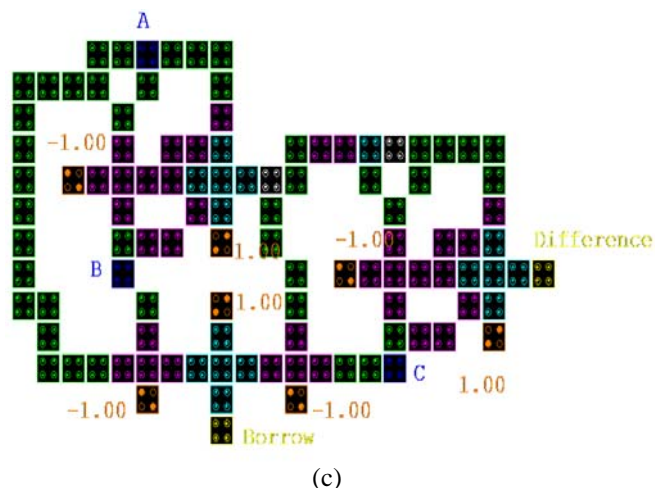

(c)

(d)

Figure 3: (a) The layout of proposed subtractor design (b) Simulation result

4. Comparison

In this section, comparison is made to other existing components with regard to various parameters. The results of the comparison of all the existing full adder and subtractor designs are presented in Table 1. The results indicate that the proposed design consumes smaller area, less clock delays and complexity as compared to the previous designs. The efficiency and robustness of these adders can verify according to area circuit complexity and clock cycles (latency). Works present in [10-14] has implement different full adder. The design needs either needs either coplanar crossovers or multiple layers to implement. We have proposed efficient full adder and subtractor, which consists of fraction of area and less circuit complexity and offer a way to implement logic and all interconnections with only one homogeneous layer of cells.

Works present in [11] consists of multiple layer to design. The proposed adder in [14] is just a handmade design. Pseudo clock zones are used. Therefore it is do not function properly. The proposed adder designs in [10] and [13] have crossover wiring that causes low robustness and fabrication difficulties in QCA circuits [24]. The proposed circuits in [13-14] are more complex and consume more area in comparison to the proposed adder in [12]. Some QCA full adders such as Zhang and Tougaw-Lent full adders occupy a large area because of using coplanar crossover connections and high cell count. crossover connections will degrade the robustness of circuits. This paper has been made is designing robust QCA structure by applying proper clock delays with less area, and complexity as [10-14].

In addition, the authors have proposed a novel full subtractor; no any comparison against QCA full subtractors

has given in open literature. The simulation results of proposed structures have been verified using QCADesigner. These novel units have been found to have less practical latency and better throughput compared to the best corresponding cases found in the literature, the circuit area is found to be reduced to a fraction of the previous noise rejecting implementations. Our aim of this paper is to design simple QCA structures with available basic gates with capable versatility and minimum garbage outputs susceptibility.

Table 1: Comparison of adder/subtractor circuits

Adders and Subtractors	Complexity (No of cells)	Area (um^2)	Latency (Clock delay)
Presented Adder in [10]	145	0.17	5
Presented Adder in [11]	220	0.36	3
Presented Adder in [12]	120	0.15	2.5
Presented Adder in [13]	180	0.22	4
Presented Adder in [14]	150	0.28	2.25
Proposed Adder fig. 3(a)	107	0.12	2.5
Proposed Subtractor fig. 4(a)	108	0.12	2.5

5. Conclusion

The main component of airthmatic logical and functional circuits are adders and subtractors. This paper presents a novel implementation of QCA full adder and full subtractor. It is inferable from the simulation results that the proposed design consumes smaller area, and offers a way to implement logic with homogeneous layer of cells. The simulation results of proposed full adder and subtractor circuits have been verified using QCADesigner. The novel units have been found to have less practical clock delay and better throughput compared to the best corresponding cases found in the literature, the circuit area is found to be reduced to a fraction of the previous noise rejecting implementations.

6. The Future Work

This paper has demonstrated the design of novel full adder and full subtractor circuits, which will be useful as an efficient building block for larger arithmetic logic units (ALU) in future. In addition, the proposed designs are a solution for minimum number of QCA cells with less crossovers. The QCA layouts and the simulation results are not only demonstrated but also analyzed for a clear understanding and facilitation of the future work.

7. Acknowledgements

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