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Efficient design for VLSI Architecture using OFDM

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M Tech (VLSI)

Abstract: ***Orthogonal Frequency Division Multiplexing (OFDM) is a system where data bits are transfer with multiple carriers and coded into a multiple sub carrier at transmission stage. Fast Fourier Transform (FFT) is widely used for operations in the field of digital technology. Some of the applications of the fast Fourier transform are as Signal analysis, Data compression, Image filtering, error free communication etc. Fast Fourier transform (FFT) is effectively use in the discrete Fourier transform (DFT) . This paper is presented the design of an OFDM Transmitter including inverse fast Fourier transform (IFFT), mapping (modulator), serial to parallel and parallel to serial converter by using VHSIC Hardware description language (VHDL). The timing simulation and synthesized results are performed and analyzed by using Xilinx ISE Project Navigator: 6.2i.***

Keywords: FPGA, OFDM, QAM, FFT, IFFT, DFT, VHDL, Communication, Power

1. Introduction

OFDM is a digital modulation technique where multiple carrier transmission, occur into a single data stream and is transmitted with low data rate. It is widely accepted for several communication purpose like Wi-Fi , Bluetooth, GPRS, Radio transmission[1] , data transfer in encrypted mode for DVB-S ,DVB-T , DVB-C, Android applications. The sub carrier-index modulation (SIM) orthogonal frequency division multiplexing (OFDM) is a recent technology that consumes less power and efficient use of bandwidth[3]. It is based on-off keying modulation to map part of the input data into the smaller part of the present sub carriers.The three basic elements in a communication system are Transmitter, Channel and Receiver. The source of information is the messages that are to be transmitted to the other end in the receiver. A transmitter can consist of source encoder, channel coder and modulation. Source encoder provides an efficient representation of the information through which the resources are conserved. A channel coder may include error detection and correction code. A modulation process then converts the base band signal into band pass signal before transmission.

2. Working

It is a combination of modulation and multiplexing signal itself is first split into independent channels, modulated by data and then re-multiplexed to form the OFDM carrier. OFDM is an advanced form of Frequency Division Multiplex (FDM). To implement the OFDM transmission scheme, the message signal must first be digitally modulated. The carrier is then split into lower-frequency sub-carriers that are orthogonal to one another. This is achieved by making use of a series of digital signal processing operations. The message signal is first modulated using a scheme such as BPSK, QPSK or some form of QAM (16QAM or 64QAM for example). In BPSK, each data symbol modulates the phase of a higher frequency carrier. The time domain representation of 8 symbols (01011101) modulated within a carrier using BPSK. In the frequency domain, the effect of the phase shifts in the carrier is to expand the bandwidth occupied by the BPSK signal to a sinc function. The zeros (or “nulls”) of the sinc frequency occur at intervals of the symbol frequency.

DFT – In DFT the computation for N-point of the DFT will calculate one by one for each point. X (k) represent the DFT frequency output at the *k*-the spectral point where *k* ranges from 0 to *N-1*. The quantity *N* represents the number of sample points in the DFT data frame. The quantity x (n) represents the *n*th time sample, where *n* also ranges from 0 to *N-1*. In general equation, x (n) can be real or complex.

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{nk}$$

IFFT -Inverse fast Fourier transform (IFFT) is used to generate OFDM symbols. The data bits is represent as the frequency domain and since IFFT convert signal from frequency domain to time domain, it is used in transmitter to handle the process.

$$x(n) = \frac{1}{N} \sum_{n=0}^{N-1} X(k) W_N^{-nk}$$

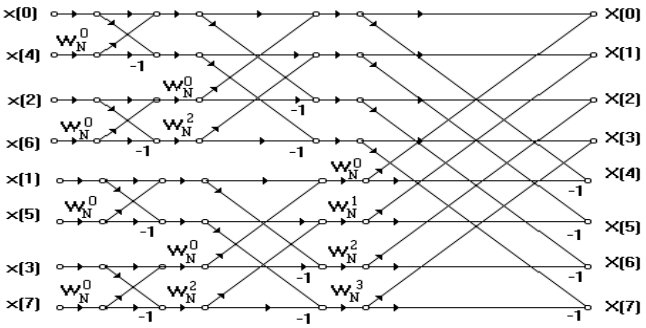

Figure 1: IFFT#

Sub carrier indexes are modulated using the On-Off keying (OOK) modulation; the carriers are modulated using standard digital modulation such as Binary Phase Shift Keying (BPSK) and M- Quadrature Amplitude Modulation (QAM) where M is in {4, 16, 64...}.Transmitted is divide into two part Book for sub carrier indexes and BQAM for carriers. The minimum number of bits of Book, corresponding to the majority bit value isN/2. In order to reduce the complexity of the transceiver, it is important to be able to send all data in BQAM.

N ∗ log2(M) −N <= (N/2) ∗ log2(M)
Where log2(M) <= 2, M <= 4

Implementation-VHDL is very adaptive, owing to its architecture, allowing designers, electronic design automation companies and the semiconductor industry to experiment with new language concepts to ensure good design tolls and data interoperability. The proposes design is implement the OFDM Sub block and finally interconnect all of them together to form complete OFDM circuit. The simulation results in Xilinx ISE Project Navigator: 6.2i

3. OFDM Transmitter Blocks

First block is the mapping block, it is the combination of (n) D flip-flop arrange in cascading form. It is first in first out approach. In proposed design n = 8, D Flip-flops for each D flip-flop input having each word (1 word =8 bit). In figure 2 and figure 3 have shown the resistor transistor logic (RTL) using 8-bit delay flip flop and 8-bit delay flip flop respectively.

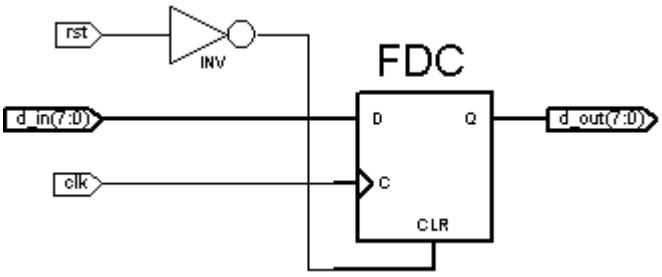

Figure 2: Resistor transistor logic (RTL) using 8-bit delay flip flop

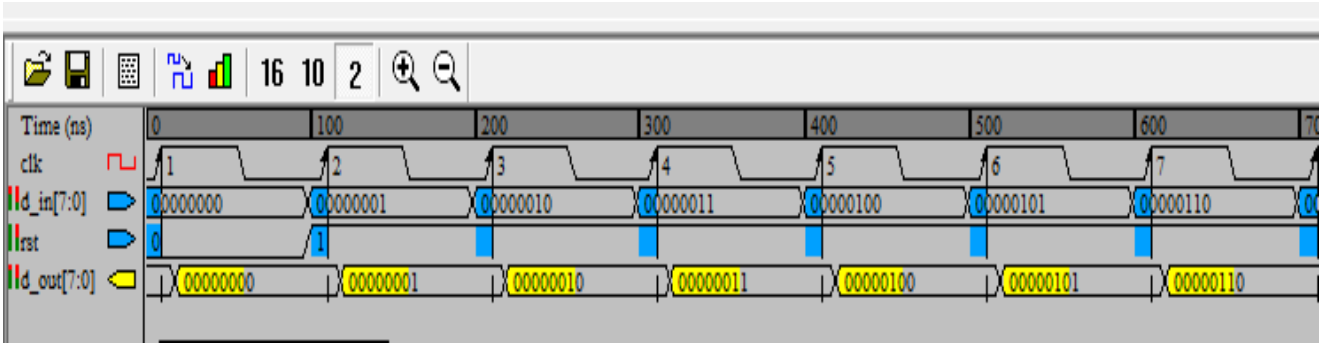

Figure 3: Output waveform of 8-bit delay flip flop#

4. Serial Input Parallel Output

Second block is the serial to parallel converter block and it is also the combination of (n) D flip-flop arrange in cascading form: Test bench waveform of serial input parallel output in proposed design n = 8, D Flip-flops for each D flip-flop input having each word (1 word=8 bit).Figure 4 shows the parallel in serial out proposed design test bench waveform

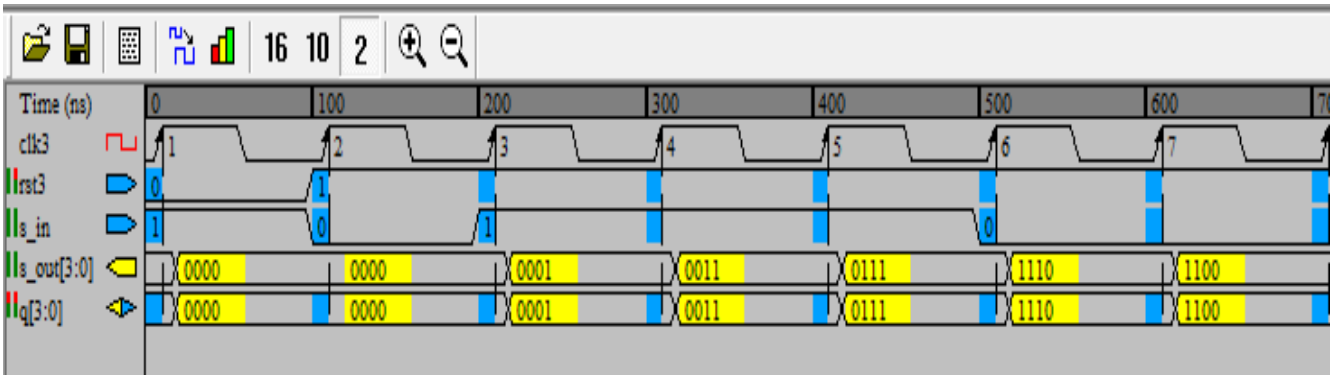

Figure 4: Output waveform of Serial Input Parallel output#

5. Final Stage

In final stage scaling is done by dividing 8 or by multiplying 0.128 with each output of stage-5. Figure 5 shows the logic diagram of stage-6, shown the resistor transistor logic (RTL) and its test bench waveform. Stage - 6 is the summation of all stages result it is the main IFFT block

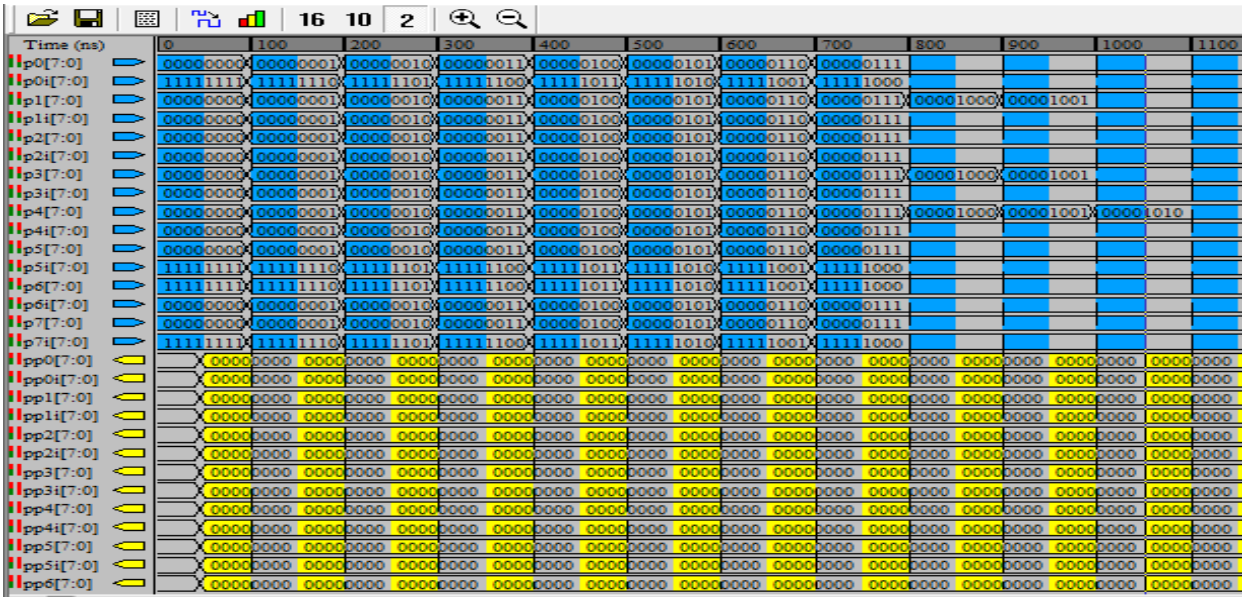

Figure 5: Test bench waveform of stage-6 of IFFT

6. Synthesized Results

Implementing the all the stage up to six stages has been captured by VHDL and the functionality is verified by RTL and gate level simulation. To estimate the timing, area and power information for ASIC design, we have used Synopsis Design Compiler to synthesize the design into gate level. Synthesized Results for stage up to six levels in IFFT.

	Number of slice	Number of Slice Flip Flops	Number of 4 input LUTs	Required time after clock (nsec)
Stage-I	116	203	256	10.752
Stage-II	101	177	256	13.991
Stage-III	195	342	256	19.382
Stage-IV	217	381	247	21.940
Stage-V	289	506	247	27.825
Stage-VI	312	618	259	30.961

7. Future Work

OFDM transmitter was successfully developed using VHDL software. Since IFFT is based on mathematical operation, MATLAB is the best platform to compare the computation result. The comparison result shows that IFFT module is working correctly as the MATLAB computation. Thus, based on the test result, it was concluded that IFFT module was mainly used in transmitter part as processing module. Thus, this module can be used as part of the OFDM system. The design can be further made to an improvement base on the suggestion.

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