The master initiates the slave read-1 command by pulling the line low and release the line. A.4. The 1-wire line is return to a logic high state through an external pull-up resistor. The master samples the line at 15us (TMSR). At this time the 1-wire line is logic high state. The master recognizes the bus status as a read-1 (time slot) request.

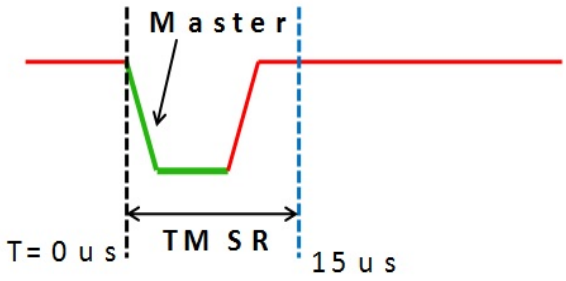

Figure 8: read-1 time slot

A.5. The master initiates the slave read-0 command by pulling the line low and it releases the line. The 1-wire line starts its internal time base at the falling edge of the master and pulls the line low for at least 15us. The master samples the line at 15us (TMSR) and recognizes the bus status as a read-0 request.

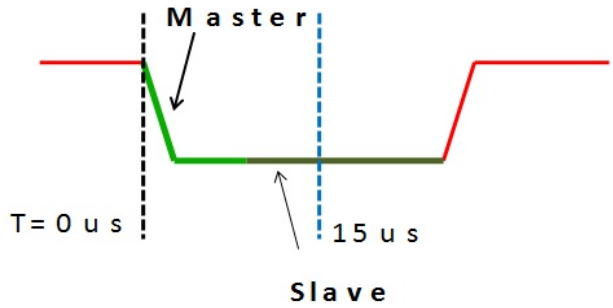

Figure 9: Read-0 time slot

The 1-wire command sequence has a three phases of transaction that begins with master generated reset sequence which is followed by the ROM command sequence in which host select its specific slave device based on its ROM ID then it perform specific device level function sequence such as write to memory or read from memory.

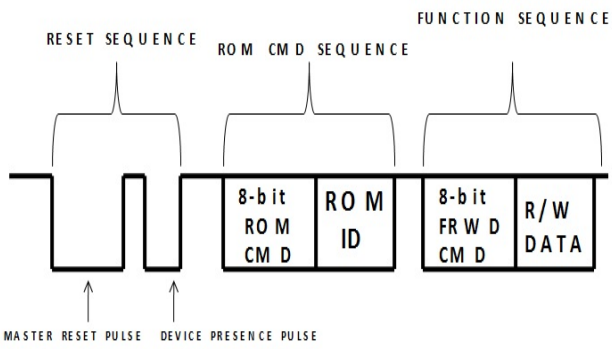

Figure 10: 1-wire command sequence

B. ROM Function Commands

Once the bus master i.e. micro controller has detected a presence of the device, it can issue one out of four ROM function commands. All ROM function commands are of eight bits long.

B.1. Read ROM [33h] or [0Fh]

Read ROM command allows the bus master to read the DS1990A's 1-byte family code, unique 6-byte serial number, and 1-byte CRC. This can only be used if there is only a single DS1990A (iButton) on the bus. If there are more than one slave is present on the bus line, a data collision will occur when all slaves try to transmit at the same time. The DS1990A (iButton) Read ROM function will occur with a command byte of either 33h or 0Fh in order to ensure compatibility with the DS1990 (iButton), which will only respond to a 0Fh command word with its 8-byte ROM data.

B.2. Match ROM [55h] / Skip ROM [CCh]

The complete 1-Wire protocol for all iButtons contains a Match ROM and a Skip ROM command. Since the DS1990A (iButton) contains only the 8-byte ROM with no additional data fields, the Match ROM and Skip ROM are not applicable which will cause no further activity on the 1-Wire bus if executed. The DS1990A (iButton) does not interfere with other 1-Wire parts on a multidrop bus that do respond to a Match ROM or Skip ROM.

B.3. Search ROM [F0h]

When a system is initially starts, the bus master might not know the number of devices on the 1-Wire bus or their 8-byte ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 8-byte ROM codes of all slave devices on the bus. The ROM search process is the continuous repetition of a simple 3-steps: read a bit, read the complement of the bit, then write the desired value of the bit which is in the complementary form. The bus master performs this simple 3-steps on each bit of the ROM. After one complete pass process, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional pass processes.

B.4. Resume ROM

Resume command is used to restart the communication with selected device.

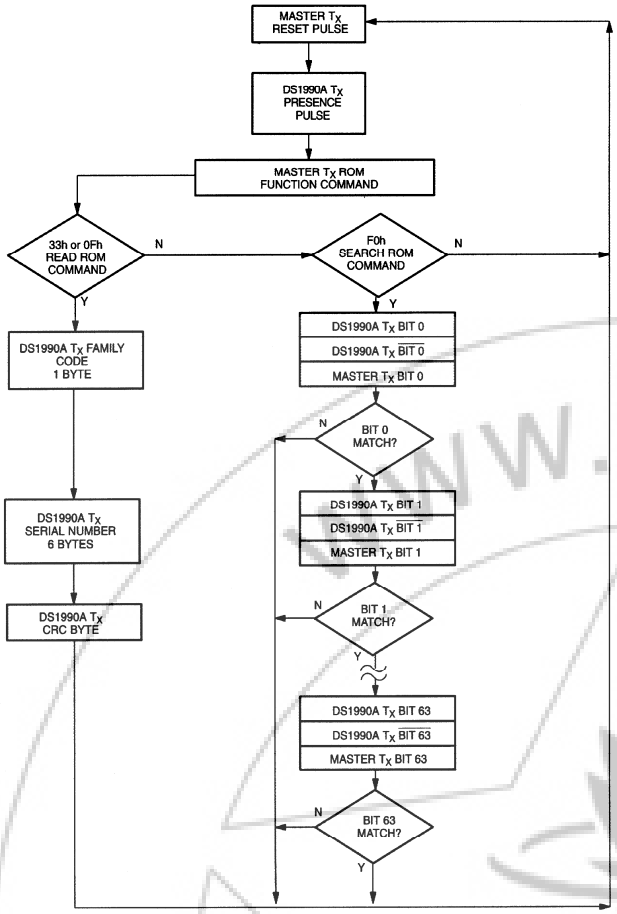

Figure 11: Flow chart of ROM function commands

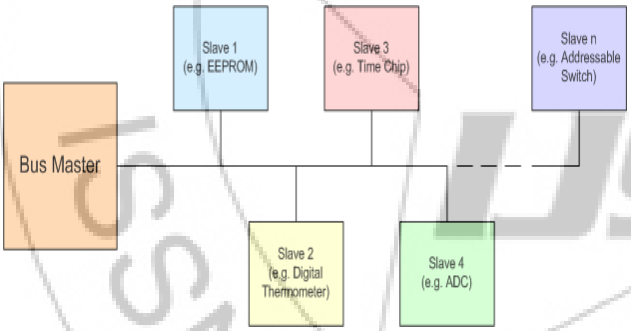

Figure 12: Connection of bus master with different slaves over 1-wire bus

4. Heart of the System 32bit Micro Controller ARM7

The LPC2148 microcontroller is based on a 32bit ARM7TDMI-S CPU that combines the microcontroller with embedded high-speed flash memory ranging from 32 kB. ARM or Advanced RISC Machine, uses a 32-bit RISC (Reduced Instruction Set Computer) processor which offers high performance and very low power consumption.

C. LPC2148 microcontroller is having following features:
C.1. The most important feature of ARM is its operating voltage is '3V to 3.6V'.
C.2. LPC2148 supports two UARTs and two fast I^2C bus (400kbit/s) which is bidirectional, for inter-IC control uses only two wires: a Serial Data line (SDA) and a Serial Clock Line (SCL).
C.3. LPC2148 has a Real Time Clock (RTC) in itself that uses a 3V reserved battery. Unlike other microprocessors, there is no need for an extra RTC IC.
C.3. LPC2148 provides two ADCs that has 2 analogy signal inputs from ADC0 and ADC1. ADC0 has 6 channels and ADC1 has 8 channels. The output is a 10-bit digital signal. It also provides one 10bit DAC that has one 10-bit digital input and one output analogy signal.
C.4. LPC2148 used two types of buses to increase the board's performance. The modules which are inside connected by the CPU high performance bus called Advance High-Performance Bus (AHB) and the peripheral are connected by VLSI Peripheral Bus (VPB). The data between the two buses are exchange at the AHB and VPB bus connection.
C.5. LPC2148 processor also employs a unique architectural strategy which is known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions. The main idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7 processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The used of Thumb instruction set can reduce the size of the control program up to 65% and increases the performance up to 160%.

C.6. LPC2148 has two types of memories such as 8 kB to 40 kB of on-chip static RAM and 32 kB to 512 kB of on-chip flash memory.
C.7. The LPC2148 is equipped with a USB device controller that enables12 Mbps data exchange with a USB host controller.
C.8. 21 external interrupt pins are available in LPC2148.

DS1990 (iButton), 1-wire bus adopted unique master-slave, bit synchronization and semi-duplex serial data transfer to communicate with ARM. The type of the pull-up resistor was decided by the number of devices and the recovery time. Generally the pull-up resistor was between 0.6 to 5KΩ.

ARM required only 1 port pin for its connection with iButton probe to which iButton DS1990 is connected shown in figure 13.

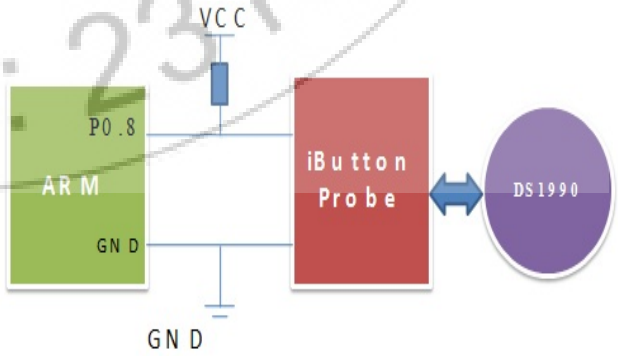

Figure 13: Interfacing between ARM iButton and ARM

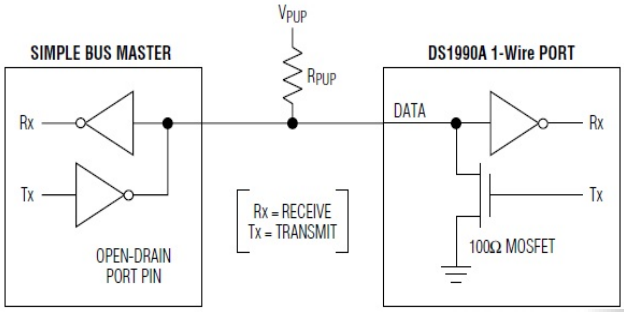

Figure 14: Equivalent circuit of ARM and DS1990A

5. Hardware Structure of the System

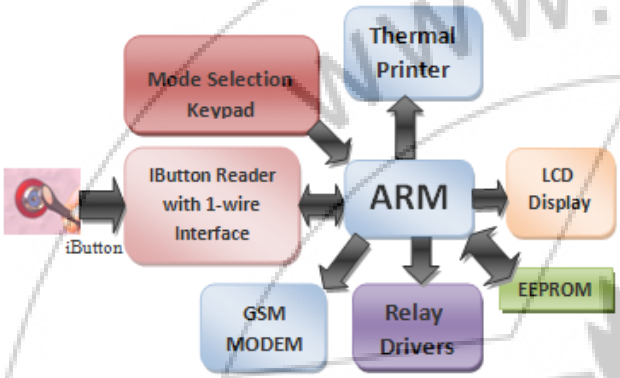

Figure 15: Hardware structure of the system

In the hardware structure, the heart of the system is ARM processor, along with the system consist of 1-wire communication device 'iButton ' with reader, external memory EEROM, motor drivers, relay drivers, GSM modem, keypad for mode selection and display unit.(figure 15). LPC2148 microcontroller is used which is of 32bit and its operating voltage is 3V.The information within the iButton can be read by an iButton reader which consists of two metal probe contacts connected to the electronic reader circuit. Whenever iButton get access to the system, then it is used for authentication purpose. For that relay drivers are used which will be responsible for opening or closing the door. Along with authentication, it is used for eCash (electronic cash) like credit cards for money transaction, petrol filling, e-toll tax and vending purpose. For permanent storage of iButton serial number, EEPROM is used. GSM modem is used for the notification purpose.

6. Conclusion

The iButton is definitely the most robust of the existing hardware token devices. Wide variety of the systems based on application of iButtons and 1-wire communication protocol have been developed and successfully implemented in various application areas. This paper proposes one more potentially very beneficial solution, where iButton electronic ID technology and 1-Wire communication protocol are employed for the multiple access such as user authentication, vending, fare collection, eCash applications such as money transaction like credit cards, swapping the card while shopping.

References

[1] WAN Jian, YUAN Yi, WANG TaiYong, "Research and Development of A Portable Data Acquisition and Analysis System Based on ARM and DSP," IEEE.2010
[2] Eugen Diaconescu, Cristian Spirleanu, "An Identifying and Authorizing Application Using 1-Wire Technology." 16th International Symposium for Design and Technology in Electronic Packaging **(SIITME)** IEEE.2010
[3] Kai-Xin Tee, Moi-Tin Chew and Serge Demidenko, "An Intelligent Warehouse Stock Management and Tracking System based on Silicon Identification Technology and 1-Wire Network Communication," Sixth IEEE International Symposium on Electronic Design, Test and Application.2011.
[4] Goran Martinovic, Tibor Kis-Konja, Zoran Kradija, "Access Control System Based On Electronic Key".
[5] www.maximintegrated.com/products/1-wire/
[6] www.maximintegrated.com/products/ibutton/ibuttons/
[7] www.maximintegrated.com/app-notes/index.mvp/id/27
[8] www.maximintegrated.com/products/ibutton/products/ ibuttons.cfm
[9] Remote Computer Interface & Security System (RCISS), Andrew Nowell, Secondary Research - iButton Security System- Page 10
[10] 1-Wire Search Algorithm, AN187, mar 2002
[11] www.keil.com/dd/docs/datashts/philips/lpc2141_42_44_46_48.
[12] www.datasheets.maximintegrated.com/en/ds/DS1990A