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Leakage Power Reduction in CMOS XOR Full Adder Using Power Gating With GDI Technique

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Abstract: ***As technology scales into the nanometre regime leakage current, active power, delay and area are becoming important metric for the analysis and design of complex arithmetic logic circuits. low leakage 1bit full adder cells are proposed for mobile application, gated-diffusion input (GDI) technique have been introduced for further reduction in power.***

Keywords: Power gating, GDI, 1-bit full adder, Sequential circuit, sleep transistors

1. Introduction

One of the most important issues in VLSI design is power consumption. With the continuously increasing chips complexity and number of transistors in a chip; circuit's power consumption is growing as well. Higher power consumption, raises chip's temperature and directly affect battery life in portable devices as it causes more current to be withdrawn from the power supply. High temperature afflicts circuit operation and reliability so requires more complicated cooling and packaging techniques.

Full adder is the fundamental unit in circuits used for performing arithmetic operations such as multipliers, compressors, large adders, comparators and parity checkers. Therefore, reducing power consumption in full adders, will reduce the overall power consumption of the whole system. Most of the VLSI application such as digital signal processing, image processing, video processing and microprocessors, extensively use arithmetic operations. Binary addition is considered as the most crucial part of the arithmetic unit because all other arithmetic operations usually involve addition. That's why, building low-power, high performance adder cells are of great interest and any modifications made to the full adder would affect the system as a whole.

One common technique for reducing power is power supply scaling. For CMOS circuits the cost of lower supply voltage is lower performance. Scaling the threshold voltage can limit this performance loss somewhat but results in increased leakages. Other techniques used in low power design include clock gating and dynamic voltage/frequency scaling. To meet the growing demand, we propose a new low power adder cell by sacrificing the MOS Transistor count that reduces the serious threshold loss problem, considerably decreasing the power consumption compared to its peer design. So now I am designing a new improved l-bit full adder cell using GDI .

The GDI cell was proposed by Morgenshteinet. a. It's a genius design which is very flexible form digital circuits. This technique optimizes the power dissipation and also reduces transistor count. The advantage of GDI technique two-transistor implementation of complex logic functions and in-cell swing restoration under certain operating conditions, are unique within existing low-power design techniques. XOR gate using GDI (gate diffusion input) technique, as it can be seen most logic functions required can be implemented using a small number of devices.

Power gating technique is use to reduce leakage current to some extent. In power gating we use sleep transistors, which is used to reduce the leakage current at pull down network. By applying fine-grain power gating approach, a "sleep" transistor is added to each and every cell, although the power of each cluster of cells is gated individually. Power gating is a modern technique that uses "sleep transistors" as high Vt devices to disconnect low Vt logic cells from the supply or ground to reduce the leakage in the sleep mode.

In this paper we will discuss two sections, first we will discuss about the previous work in section 2, and then we will discuss the proposed work under section 3 in which we will use both the technique GDI and Power gating in a sequential 1-bit full adder.

2. Previous Work

Fig.1 shows the conventional CMOS 28 transistor adder. This is considered as a Base case throughout this paper. All comparisons are done with Base case. The CMOS structure combines PMOS pull up and NMOS pull down networks to produce considered outputs. Transistor sizes are specified as a ratio of Width/Length (W/L). The sizing of transistors plays a key role in static CMOS style. It is observed in the conventional adder circuit that the transistor ratio of PMOS to NMOS is 2 for an inverter and remaining blocks also followed the same ratios when we considered the remaining blocks as an equivalent inverters. This ratio does not give best results with respect to noise margin and standby leakage power when it is simulated in 90nm process. Modified adder circuits with sizing are targeting the noise margin, and ground bounce noise.

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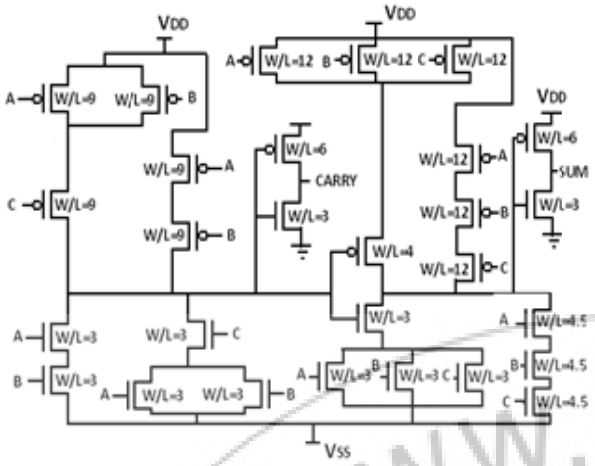

Figure 1: Conventional CMOS full Adder

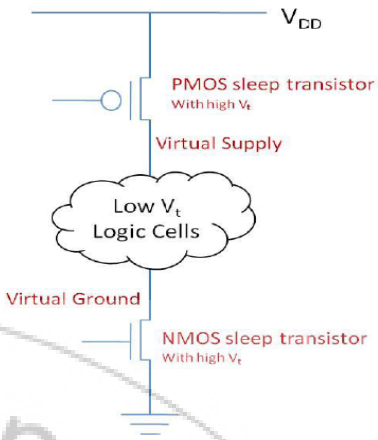

Figure 2: Power Gating

In previous work, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that output levels can be no higher than the input level. Each transistor in series has a lower voltage at its output than at its input. If several devices are chained in series in a logic path, a conventionally-constructed gate may be required to restore the signal voltage to the full value. By contrast, conventional CMOS logic always switches transistors to the power supply rails, so logic voltage levels in a sequential chain do not decrease. Since there is less isolation between input signals and outputs, designers must take care to assess the effects of unintentional paths within the circuit. For proper operation, design rules restrict the arrangement of circuits, so that sneak paths, charge sharing, and slow switching can be avoided. Simulation of circuits may be required to ensure adequate performance.

3. Proposed Work

Power gating technique is used to reduce the leakage power, where a sleep transistor is connected between actual ground rail and circuit ground. Ground bounce noise is being estimated when the circuits are connected with a sleep transistor. Further, the peak of ground bounce noise is achieved with a proposed technique

3.1 Power gating

An additional sleep transistor is add to the pull up or to the pull down network. Larger sized devices are useful only when interconnect dominated. Minimum sized devices are usually optimal for low-power. Glitches causes spurious transitions, gates have nonzero delay, Glitches due to mismatch in path lengths of circuit.

Glitches can be eliminate using insertion of buffers to equalise gates path lengths or we can redesign the circuit.

3.2 Sequential circuit with header and footer using GDI implementation

Using GDI technique we can optimizes the power dissipation and also reduces transistor count.

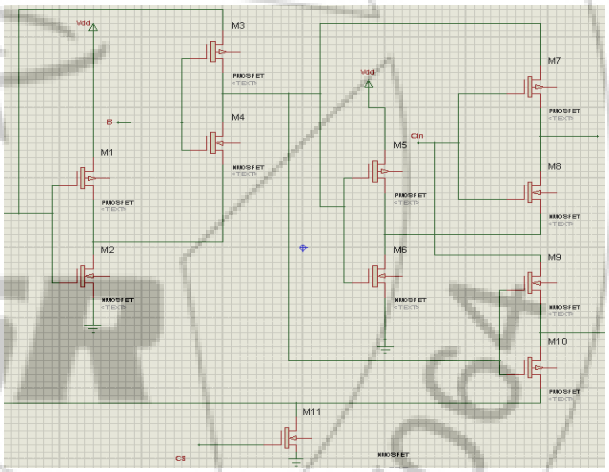

Figure 3: 1-bit Full Adder GDI Design using Footer(sleep transistor)

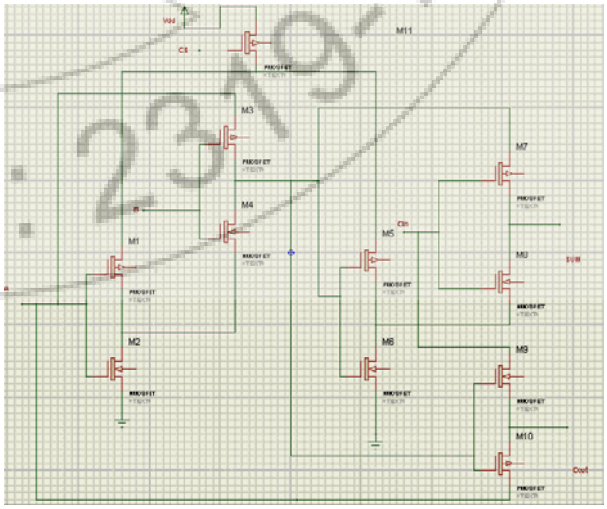

Figure 4: 1-bit Full Adder GDI Design using header (sleep transistor)

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The PMOS and NMOS Transistors used as header and footer are high **Vt** transistors as compared to other transistors in the circuit.

4. Result and Comparison

In this paper we used GDI and power gating technique in a sequential circuit, if we did not use this technique than it is not possible to reduce the power consumption to that level.

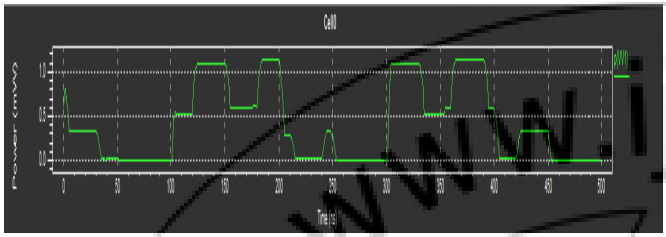

Figure 5: Power waveform of sequential circuit when apply header and footer

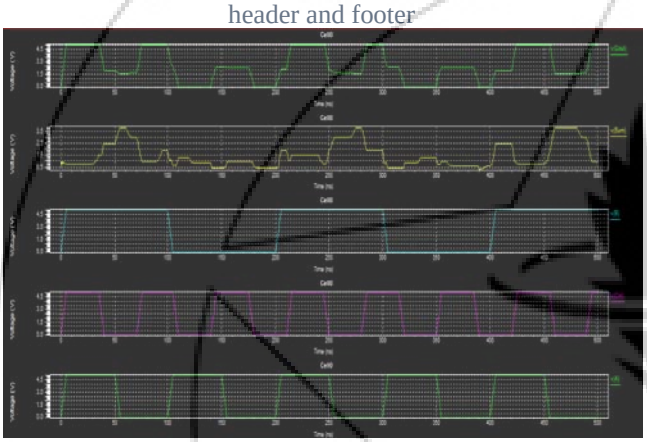

Figure 6: Voltage waveform of sequential circuit when apply header and footer

Here we took 2.5 voltage source and the power difference between the conventional and proposed design is 5.6763e-003 mW.

Table 1: Comparison table

Design	Power(mW)
Conventional full adder	6.9297
Full Adder Using GDI	2.9401
Full adder with footer (Power gating)	2.6453
Full adder with Footer and header(power gating)	1.2534

5. Conclusion and Future Scope

In this paper, 1bit full adder is implemented using GDI Technique and power gating. This method could apply on combinational or sequential circuits. Proposed work is for minimizing the power consumption and delay timing so that it is better to use the module in future those can work on less power. This can reduce cost. In gating we used cell which also consumes power and some time.

We will observe that “52.65%” of power get reduced, we can reduce the time up to “74.4%”. Combining power gating is convenient when the energy necessary to reactivate the circuit is smaller than the leakage energy consumed by the circuit in the idle state. We can implement the circuit by using other tool like Xlinix and Cadex, and it is also possible to reduce delay time by reducing the number of transistors, our work also get implement by reducing the size of the wire used in then circuit.

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References

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