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Design of 1.8V, 72MS/s 12 Bit Pipeline ADC in 0.18µm Technology

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Abstract: ***This paper presents 12 bit pipeline ADC designed for the implementation of pipeline analog to digital converter. Designing includes TIQ comparator that reduces area and power consumption on a single chip. The general guideline is to design high speed, low power pipeline ADC with wide input bandwidth. Each block is designed at transistor level and design is simulated and verified on LT SPICE SWITCHER CAD-III schematic editor simulation tool using 0.18µm technology. The simulation result shows that Sampling Speed is 72MS/s with power dissipation of 7.66 mW with power supply having 1.8V.***

Keywords: Single stage pipeline ADC, TIQ comparator, Sample and hold, high speed, low power**.**

1. Introduction

The analog-to-digital converter (ADC) is an essential part of system-on-chip (SOC) Products as it bridges the gap between the analog physical world and the digital Logical humankind. Here in the study, The Pipelined Analog-to-digital converter (ADC) has become the most popular ADC architecture for sampling rates from a few mega samples per second (Msps) up to 100Msps+. Resolutions range from twelve bits at the faster sample rates awake to 16 bits at the inferior rates. These resolutions in addition to sampling paces cover a wide assortment of relevance's, as well as CCD imaging, ultrasonic therapeutic imaging, digital recipients, base stations, digital video (for example, HDTV), xDSL, cable modems. The design pipe line ADC implemented in TIQ technique used ascomparator. The proposed pipeline ADChere has been developed for better implementation in high speed applications in communication systems. Four issues have been taken to achieve high speed, low power consumption, and low voltage operation in the pipe line ADC. Here transmission gate uses as a sample and hold circuit and DAC uses as a multiplexer.

The proposed ADC utilizes the Pipeline ADC technique that uses 2 bit internal flash which have provided high resolution, high sampling rates, low power dissipation and high throughput.

The Pipeline ADC architecture involves sample-and-hold(S/H), N-bit Flash ADC, subtractor, reconstruction DAC, residue amplifier. In Figure 1, the analog input Vin is first sampled and held steady by sample-and-hold(S/H). The Flash ADC in stage 1 quantizes to two bits. The 2-bit output is fed to two inputs DAC.

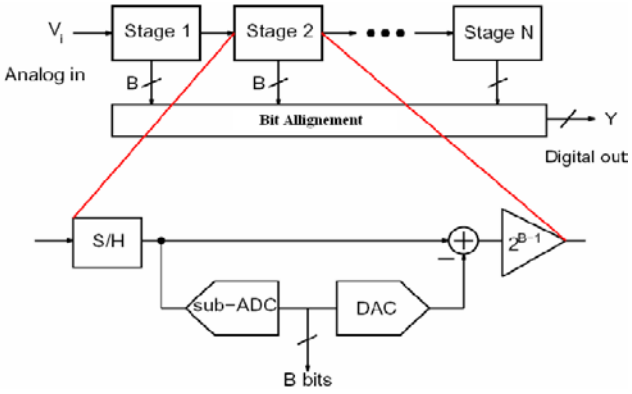

Figure 1: Block diagram of Pipeline ADC

The output of DAC is subtracted from the input. This residue is gained up and then fed to next stage of pipeline block. As bits from each stage are determined from different points so all the n –bit digital outputs are combined using shift registers and digital error correction logic [1].

2. Design and Implementation

2.1 Design of Single Stage

Flash ADC provides high throughput so pipeline ADC stages are inherited from Flash architecture. The number of comparators will be decided on the basis of resolution of each stage of pipeline ADC. In 12-bit pipeline ADC, design is implemented using 2 bit per stage, so total no of stages will be six. The number of comparator required in each stage will be $(2^2 - 1)$ that is 3 comparators will be used in single stage. Figure 2 shows architecture of single stage pipeline ADC.

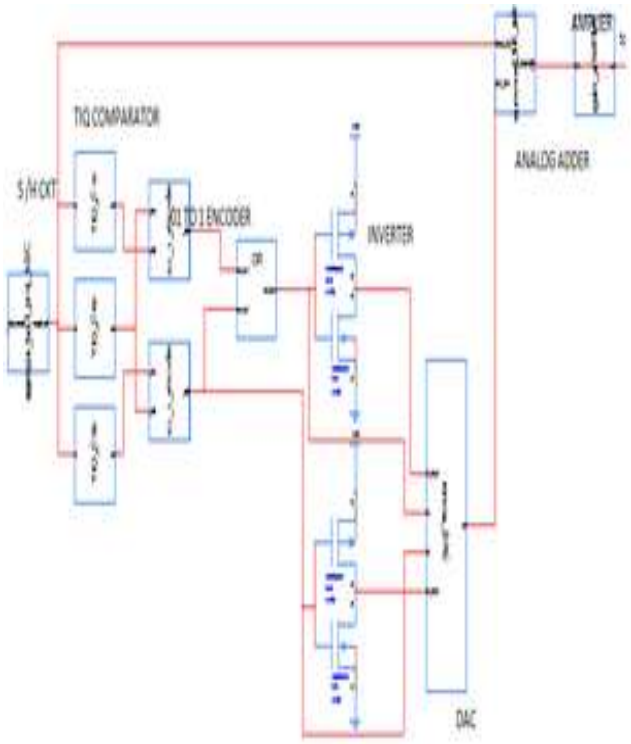

Figure 2: Single Stage Pipeline

For design of single stage of pipeline ADC, the required components are:

- Sample and Hold(S/H)
- TIQ comparator
- TC to BC encoder
- 2-bit Digital to Analog converter
- Operational amplifier

2.2 Design of Sample and Hold Circuit

Sample-and-hold circuitry is necessary for ADC front-end circuits to allow the ADC to track and then hold the inward bound signal. Once the signal has been tracked, the ADC throws a switch to disconnect the input signal from the front end; it then holds that input signal level as long as enough for the ADC to complete its conversion cycle. These sample-and-hold or T/H circuits possess considerable bandwidth to allow the ADC to track high input frequencies. They must remain linear over this wideband width, which requires excellent design techniques to provide the high bandwidth without adding unnecessary noise coupling. The switch and hold capacitors must charge up and hold the signal representation for considerable times to allow the ADC quantizer to accurately estimate the changing input signal amplitude. The sampling CLK is known to the control of the Transmission gate. When CLK is high the input signal is sampled from first buffer and the capacitor is charged to the input level. When CLK goes to LOW, then the path from the input is open circuited and the sampled voltage is maintain constant and given to the previous block for conversion. For a better sampling the sampling rate should be at least 2 times to that of the input frequency [2].

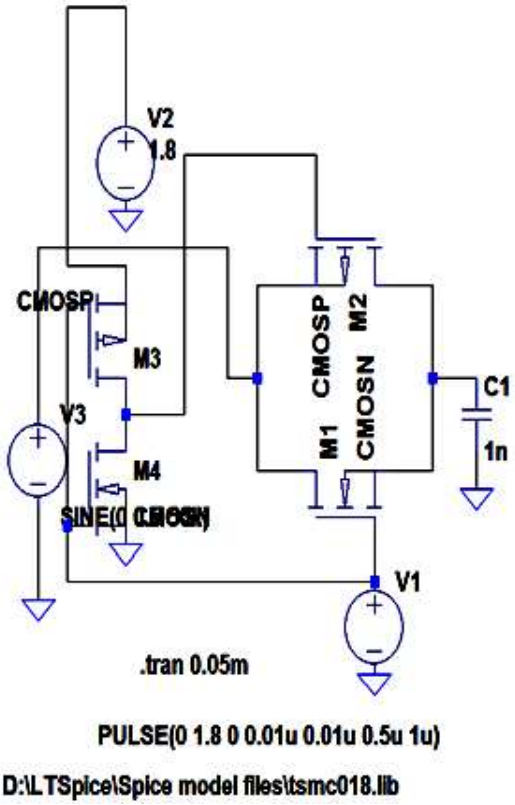

Figure 3: Schematic diagram of Sample and Hold

The sampling period is kept small as compared to holding period; this is kept so that the output of the OPAMP will get settled, two clocks of same period but no overlapping in nature are used one for sampling the analog voltage and other is used to latch the converted data. This method is chosen because, if the output is directly taken from the comparator (see figure 3) the output of ADC will oscillate and so that output of DAC which will result in cumulative error and thus a flip-flop is put in front of comparator so as to convert the settled value from S/H amplifier.

2.3 Design of TIQ Comparator

Implemented ADC features the Threshold Inverter Quantization (TIQ) technique for design of high speed and low power ADC using standard CMOS technology. The make use of cascade inverters at the same time as a voltage comparator is the reason for the procedure's name. The voltage comparators measures input voltage with internal reference voltages, which are find out through the transistor dimensions of the inverters. A few numbers of the foremost problems of the usual comparator structure used in ADC designs are large transistor area for higher accuracy, DC bias requirement, charge injection errors, high power consumption. In this case BICMOS technology would be necessary to integrate both a high-speed conversion and low-power dissipation [3].

Looking at the transfer characteristics of inverter we well find that this seems to behave as comparator. This design also saves the requirement of reference generator and the comparator will much quicker than the conventional comparator because it requires only 4 transistors (first one to locate the requisite threshold voltage and next one to get requisite gain and avert unbalanced propagation

impediment). Mathematically the value of threshold voltage is governed by means of Equation 1.

$$Vt = \frac{r(Vdd-Vtp)+Vtn}{1+r} \ldots\ldots (1)$$

$$\text{wherer} = \sqrt{\frac{Kp}{Kn}}$$

Where, Vt =threshold voltage of inverter
Vtp, Vtn = threshold voltage of PMOS and NMOS respectively.

From the Technology Model File, the important parameters are:
Kn=64.9µA/v2,Kp=18.77µA/V2,Vtn=0.678V,Vtp=0.6722V, µn=417.4cm²/v.s, µp=121.3cm²/v.s, n=0.02, p=1.04

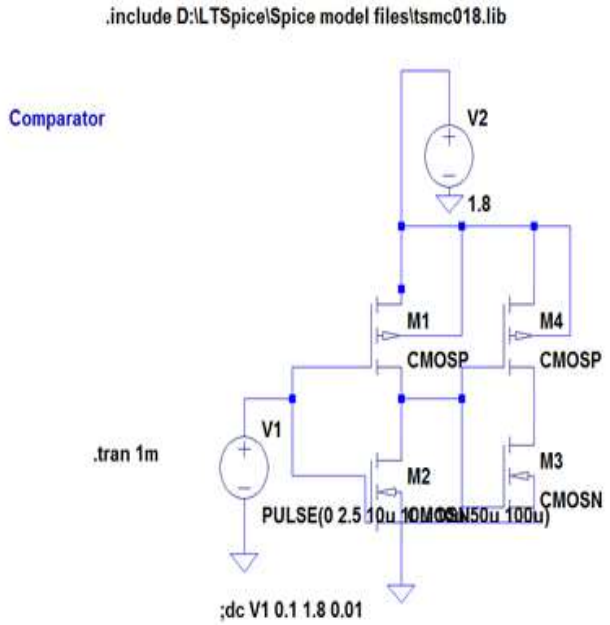

Figure 4: Schematic diagram of Comparator

We have implicit that both transistors are in the active area the gate oxide width (Cox) for both transistors will be the same, and the lengths of both transistors (Lp and Ln) will be same.

Expanding equation

$$Vt = \frac{\sqrt{\frac{\mu pWp}{\mu pWn}}(Vdd-Vtp)+Vtn}{1+\sqrt{\frac{\mu pWp}{\mu pWn}}} \ldots\ldots (2)$$

Where µp and µn are the electron and hole mobility.

Since, in the projected architecture three comparators are requisite. So we have to design three comparators to get their threshold voltages.

2.4 Design of Two Stage Operational Amplifier (OPAMP)

Operational Amplifiers are the backbone for many analog circuit designs. The speed and accuracy of these circuits always depends on the bandwidth and DC gain of the Op-amp, the implementation of a CMOS OPAMPs that combines a considerable dc gain with higher unity gain frequency has been a most difficult problem. There have been several circuits proposed to evaluate this problem. The purpose of the design methodology in this paper is to propose accurate equations for the design of high- gain 2-stage CMOS op-amp.

Its main drawback is the non-dominant pole formed by the load capacitance and the output impedance of the second stage, which reduces the achievable bandwidth. Another potential disadvantage is the right half plane zero that arises from the feed forward signal path through the compensating capacitor.

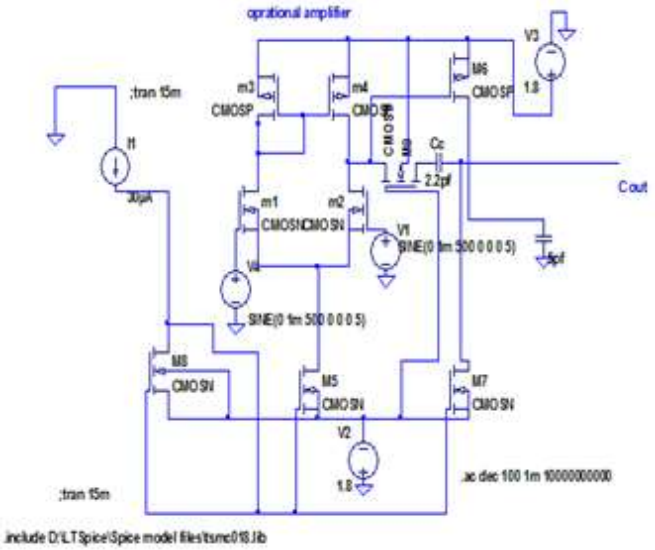

Figure 5: Schematic of Two Stage Operational Amplifier

Based on the clear understanding of different specifications, the standard CMOS OPAMP circuit topology has been implemented

Table 1: Specification of two stage CMOSOPAMP

Specification	*Values*
Supply Vdd	1.8V
Gain	≥60db
Gain bandwidth	4MHZ
Settling time	1µs
Slew Rate	10V/µsec
Input common mode	(-1V)-2V
Common mode rejection	≥60db
Output swing	1-2.4V
Offset	≤10m

2.5 Design of 2-Bit DAC

There are different configurations that can be used to design digital to analog converter (DAC) similar to resistor hierarchy (voltage separator architecture), charge division rule, current division architecture and many others, but all of this uses lot many components and complex in nature. Thus to digital CMOS technology, multiplexer logic has been employed to act as DAC, since the purpose of DAC is to provide an analog voltage corresponding to digital bits, as shown in table 1.

Table 2: DAC output at different stages

Digital bits S1S2	*Reference*	*Transistor*	*Voltage (V) (OUTPUT)*
00	Vref1	M1 & M2	0
01	Vref2	M3 &M4	0.45
10	Vref3	M3 & M5	0.9
11	Vref4	M4 &M6	1.355

That means a effortless analog multiplexer can do this trade the logic equation recitation the procedure of the Multiplexer that we are using here as a 2-DAC.Figure 6 shows the circuit of analog multiplexer. In a multiplexer there are many inputs and only one output. So in this proposed work, each stage consists of a 2 bit so there are 4:1 multiplexer is required the operation is as follows – if "S0 S1" Is zero then M1 & M2 is on so "Vref1" is passed and we will get analog value 0v.If S1=0,S=1,then M3 & M4 Transistor are on so Vref2 is passed then we will get analog value 0.45v, if S1=1,S2=0, then M2 & M5 are on so "Vref3" is passed then we will get analog value 0.9v. If S1=1,S2=1, then M4 & M6 are on so "Vref4" is passed then we will get analog value 1.355v.

The reference voltages are generated with the help of a simple resistor divider network with two supplies at either end of the resistor divider, which is having similar working like active ladder network. The active resistor is a MOS connected in diode configuration, i.e. drain is connected to gate and source to substrate. The reference voltages are generated with the help of a simple resistor divider network with two supplies at either end of the resistor divider, which is having similar working like active ladder network The active resistor is a MOS connected in diode configuration, i.e. drain is connected to gate and source to substrate.

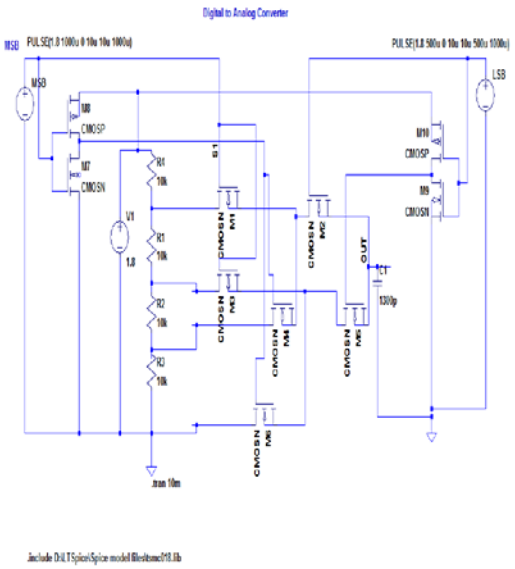

Figure 6: Schematic Of 2-Bit DAC

3. Simulation Results

This section clearly discusses the simulation results of above said different important blocks of pipeline ADC. This work is carried out on LT SPICE CAD-III and simulation is carried out using 0.18µm technology. The schematic of TIQ comparator, sample-and-hold, operational amplifier, DAC and D flip-flop are simulated.

3.1 Result of Sample and Hold

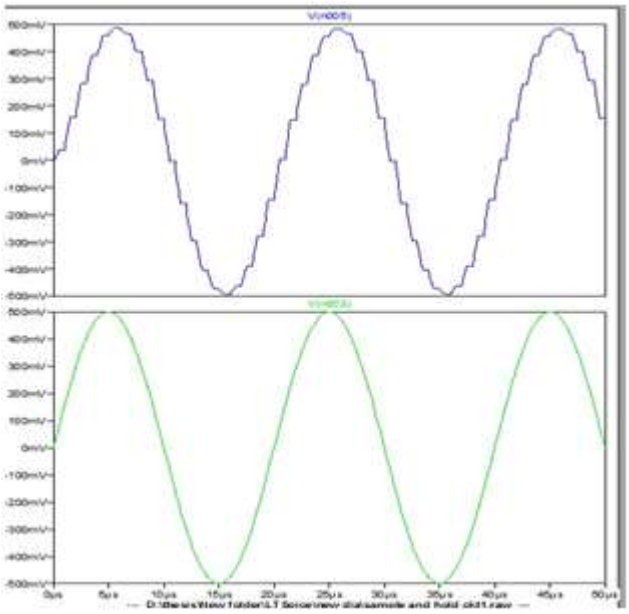

Figure 7: Output waveform of Sample and Hold

3.2 Result of Comparator

In DC analysis result of a comparator, reference is set to 0.9v.

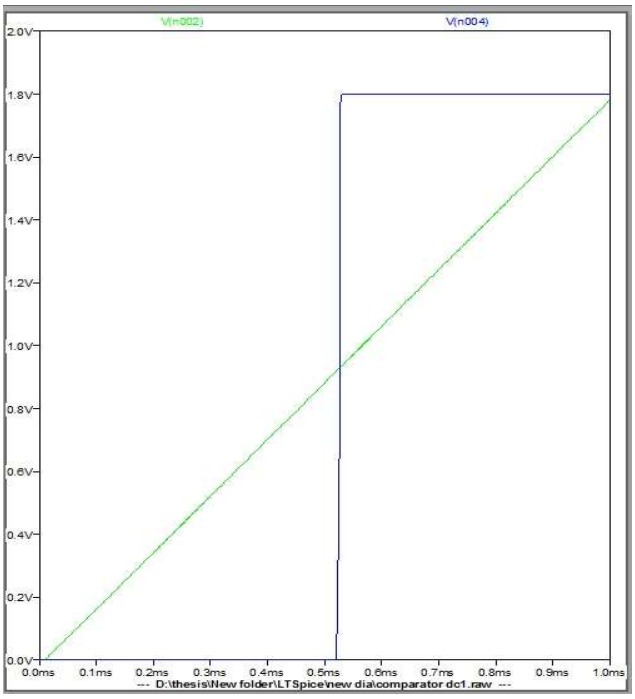

Figure 8: DC sweep waveform

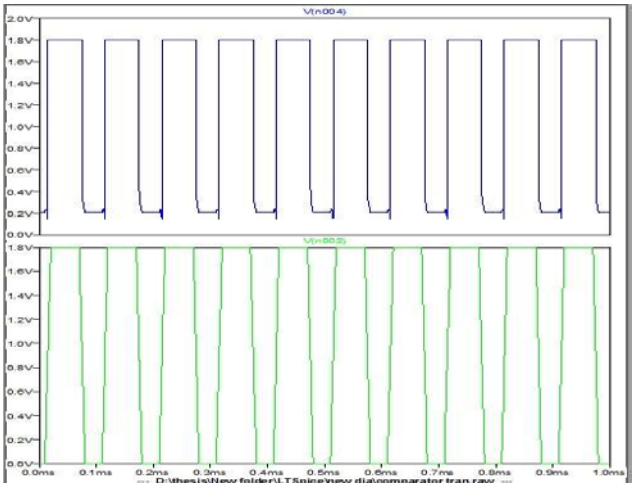

Figure 9: Transient curve of Comparator

3.3 Result of OPAMP

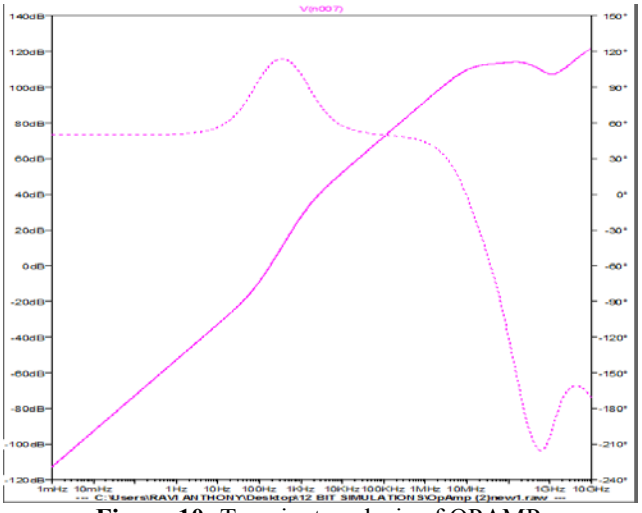

Figure 10: Transient analysis of OPAMP

3.4 Result of 2 bit DAC

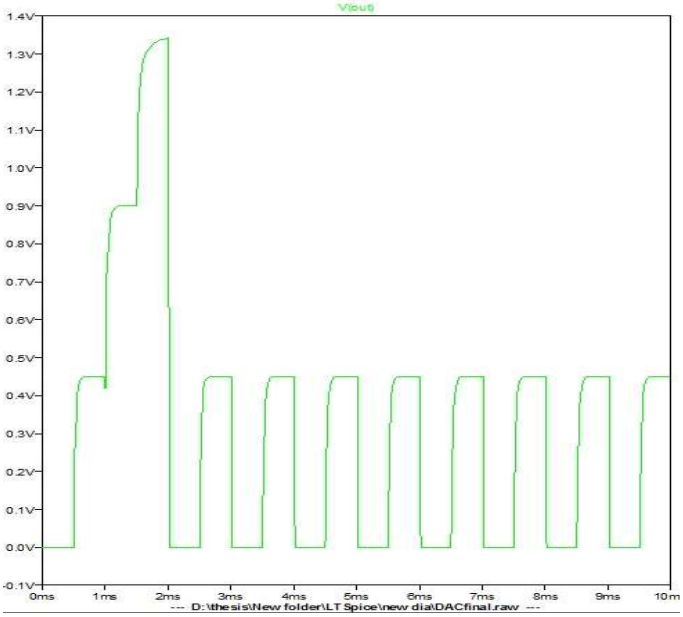

Figure 11: Output of DAC

3.5 Result of 12 Bit Pipeline ADC

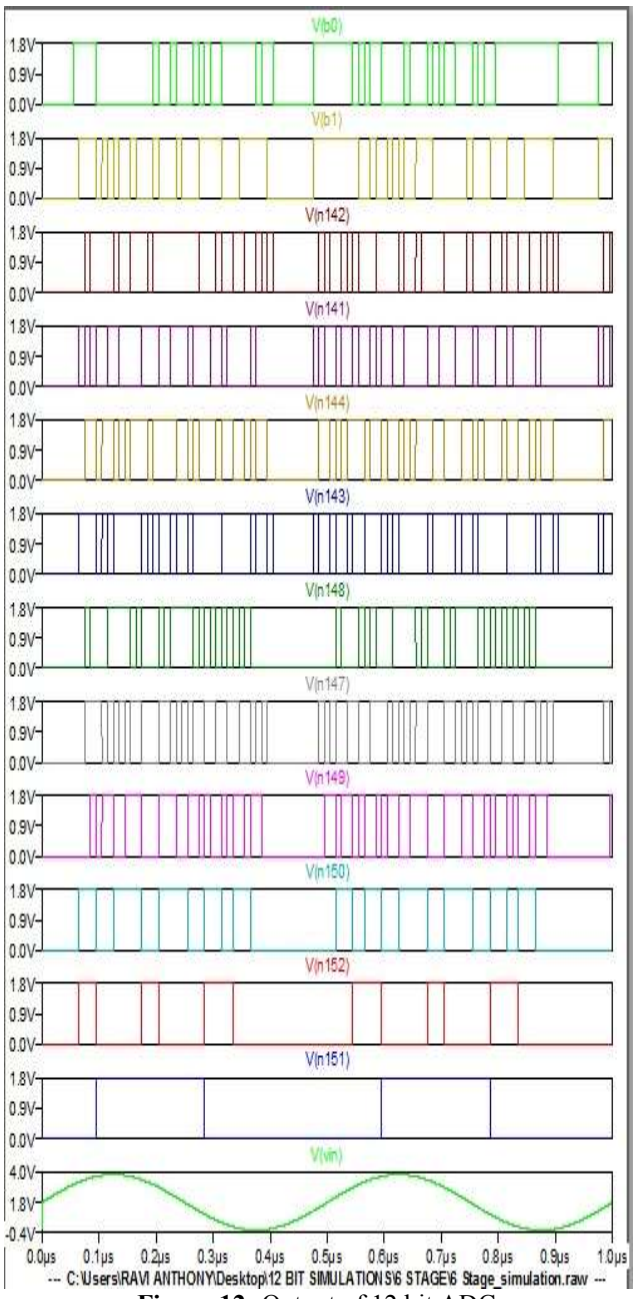

Figure 12: Output of 12 bit ADC

Table 3: Parameter Values

S. No	*Name of Parameters*	*Proposed design*
1	Resolution	12bit
2	comparator	3
3	Gain	73.38dB
4	Power dissipation	7.66mW
5	technology	0.18µm
6	Power supply	1.8V
7	Bit/stage	2

4. Conclusion

12 Bit Pipeline ADC design has been implemented and verified on LT SPICE SWITCHER CAD III using 0.18µm technology. This Pipeline is operated at power supply voltage of 1.8v and design architecture is found to consume 7.66mw power with gain 73.38dB.

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