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Study and Analysis of Power Dissipation and Different Operational Amplifier (Op-Amp) Parameters of BJT (741) Op-Amp and CMOS Op-Amp Using T-SPICE

Ashish Kumar Singh[1], Nidhi Goyal[2]

[1]M. Tech student, Department of ECE, Gyan Vihar School of Engineering and Technology, SGVU, Jaipur, Rajasthan, India

[2]Assistant Professor, Department of ECE, Jagannath Gupta Institute Engineering of Technology, Jaipur, Rajasthan, India

Abstract: ***An operational amplifier ("op-amp") is a DC –coupled high gain electronic voltage amplifier with a differential input and, usually a single-ended output. We can design operational amplifier using bipolar junction transistor (BJT) technology and Complementary metal oxide field effect transistor (CMOS) technology. BJT is the fastest technology and CMOS is the lowest power consumption technology. In this analysis I will cover various aspects of an op-amp like power consumption, offset voltage for small signal and large signal mode, input bias current, input offset current, gain and frequency response, maximum and minimum output voltage swing, slew rate etc. Operational Amplifier is important building blocks for a wide range of electronic circuits.***

Keywords*:* operational amplifier, slew rate, power consumption and T-spice.

1. Introduction

I choose op-amp so I can deeply understand the several parameters of op-amp and tried to improve them for future use. In this work I first analyzed the parameters of op-amp using bipolar junction transistor **(BJT)** and then I analyzed and calculated that same parameters of op-amp circuit using Complementary metal oxide semiconductor **(CMOS).** These circuits will be simulated on T-Spice and then performed a healthy comparison between all the parameters which I have found. In some cases BJT has better performance and in some cases CMOS has better performance.

So at last I deeply analyzed all the important parameters which play the important role in the performance of op-amp for industrial and scientific purposes and reached to a result that where power and slew rate factor matters more than some other factors then we come o the CMOS which consumes very low power and has very good slew rate (rate of change of output according to input) but where speed is the major concern than BJT is the better option.

The design of an integrated circuit **(IC)** requires a different approach. Due to the minute dimensions associated with the IC, a bread boarded version of the intended circuit will bear little resemblance to its final form. The parasitic components that are present in an IC are entirely different from the parasitic components present in the breadboard, and signal measurements obtained from the breadboard usually do not provide an accurate representation of the signals that appear on the IC.

2. Tanner Tool

Spice is a general purpose circuit simulator capable of performing three main types of analysis: nonlinear DC, nonlinear transient and linear small-signal AC circuit analysis. Nonlinear DC analysis or simply DC analysis, calculates the behavior of the circuit when a DC voltage or current is applied to it. In most cases, this analysis is performed first. The result of this analysis is commonly referred to as the DC bias or operating-point characteristic. The Transient analysis, probably the most important analysis type, computes the voltages and currents in the circuit with respect to time. The third type of analysis is a small-signal AC analysis. It liberalizes the circuit around the DC operating point and then calculates the network variables as functions of frequency.

The T-Spice user interface consists of the following elements:

- Title bar
- Menu bar
- Toolbars
- Status bar
- Simulation Manager
- Simulation status window

3. OP- AMP Circuit Using BJT and CMOS

I have done simulation of two circuits of operational amplifiers using BJT and CMOS.

A. Op-amp circuit using BJT

A detailed circuit schematic of the 741 op amp which I have used in all my analysis is shown in figure 1. It consists of five main parts. These are bias current, input gain stage, second gain stage, output buffer and short-circuit protection stage.

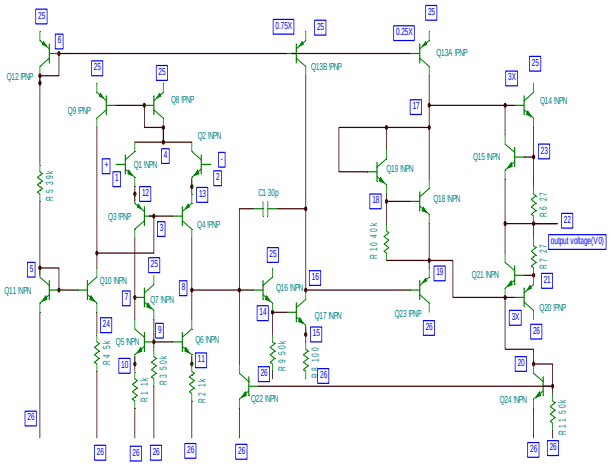

Figure 1: 741 operational amplifier circuit using BJT

B. Op-amp circuit using CMOS

Figure 2 shows the two stage CMOS operational amplifier circuit. It contains the few NMOS and PMOS transistors, some resistances and some capacitances. Now next I find out the all parameters of the CMOS and BJT Op-amp both circuits and then I will compare all the calculated parameters of both op-amp circuit. We will simulate CMOS and BJT Op-amp circuit using T-Spice.

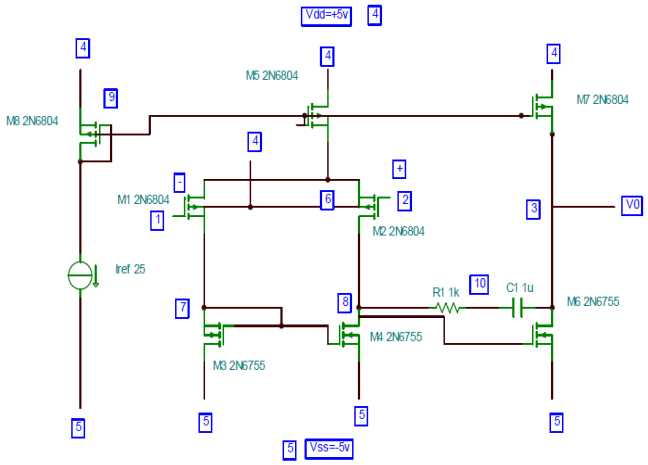

Figure 2: Two stage CMOS op-amp circuit

4. Parameters of OP- AMP Circuit

In this paragraph I will perform a detailed Spice analysis of the 741 op-amp circuit at the transistor level, including an investigation into its static and dynamic circuit behaviors. Then I will show a CMOS op-amp design that is finding important applications in VLSI systems.

A. *Detailed analysis of 741 op-amp circuit*

We find the different op-amp parameters value using T-SPICE with waveforms for 741 op-amp circuit. These are:

- DC voltage gain

We obtained from graph, linear region is from -359.89 micro volts to -268.44 micro volts this corresponds to maximum output voltage swing bounded from -13.28 volts to +13.18 volts. This graph is shown in figure 3. DC voltage gain is **2.893×10^5.**

- DC Offset voltage

It is the voltage actually where output voltage tends to zero. Here the transfer characteristics of this amplifier cross the 0v output axis somewhere between -320 micro volts to -310 micro volts. A closer look and careful look using probe indicated that the crossover point occurs at **-3.1183×10^{-4}V.** This is shown also in figure 3.

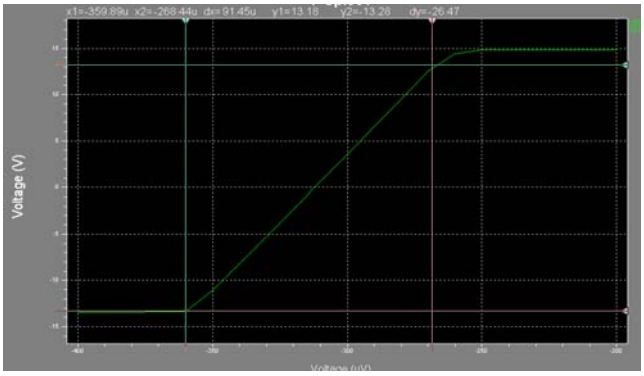

Figure 3: Transfer characteristics of 741 op-amp circuit

- Input bias current (I_B)

Other DC information, such as input bias current, static power dissipation, and so on, was calculated through **.OP** command. We can then repeat the DC analysis with the following element statement.

V_d 101 0 DC -311.83μV

So the input bias current (I_B) can be calculated from simulation as

$I_B = I_{B1}+I_{B2}/2$
$I_B = ((34.2 \times 10^{-9}A) + (34.4 \times 10^{-9}A)) / 2$
$I_B = 34.3 \times 10^{-9}A$

- Input offset current (I_{io})

The input offset current can be calculated with the help of difference of two currents.

$I_{io} = I_{B1}-I_{B2}$
$I_{io} = (34.2 \times 10^{-9}A) - (34.4 \times 10^{-9}A)$
$I_{io} = 0.2 \times 10^{-9}A$

- Power dissipation (P_d)

The total power dissipation can be calculated by P=V×I. Here current at Power supply is from +15 volts to -15 volts that is equal to 30 volts and current at V_{cc} is 18.398×10^{-4}so power can be calculated as:

$P_d = V \times I$
$P_d = 30 \times 18.398 \times 10^{-4}W$
$P_d = 5.5194 \times 10^{-2}W$

- Slew rate (SR)

It is defined as the maximum rate of change output voltage per unit of time and is expressed in volts per millisecond. In equation form

SR= dV_o / dt maximum V / microsecond.

The positive-going slew rate is estimated at +0.544 V/micro second. The negative-going response behaves in a more expected way, showing a steady decline from +5V to -5V. The negative-going slew rate is found to be -0.313 V/micro second, which are shown in figure 4.

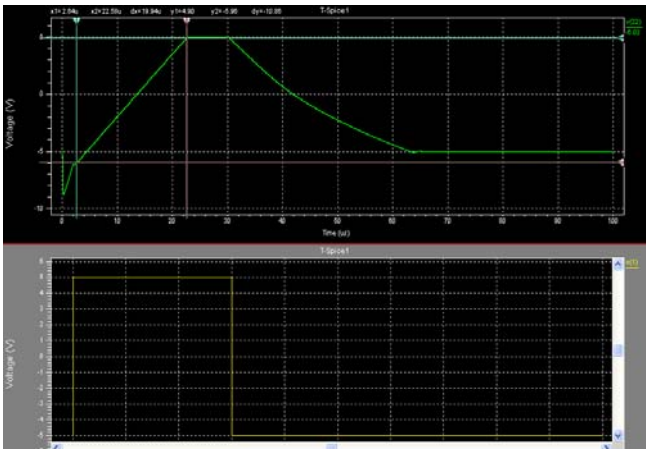

Figure 4: Slew rate waveform of 741 op-amp circuit

B. Detailed analysis of CMOS op-amp circuit

We find the different op-amp parameters value using T-SPICE with waveforms for CMOS op-amp circuit. These are:-

- DC voltage gain

We obtained from graph, linear region is from -9.18×10^{-4} V to $+11.9 \times 10^{-4}$ V this corresponds to maximum output voltage swing bounded from -4.74V to +4.58V.This graph is shown in figure 5. DC voltage gain is **44.213×10^{2}.**

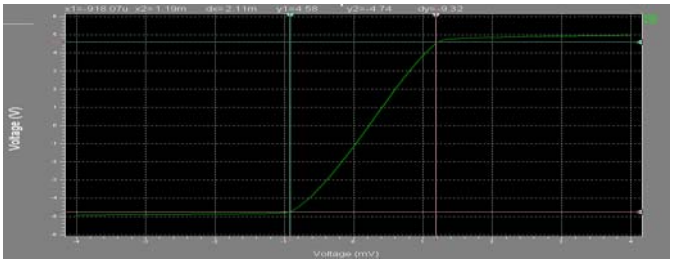

Figure 5: Transfer characteristics of CMOS op-amp circuit

- DC Offset voltage

It is the voltage actually where output voltage tends to zero. Here the transfer characteristics of this amplifier cross the 0v output axis somewhere between -215 micro volts to -225 micro volts. A closer look and careful look using probe indicated that the crossover point occurs at **-2.1517×10^{-4}** volts**.** This is shown also in figure 5.

- Input bias current (I_B)

Other DC information, such as input bias current, static power dissipation, and so on, was calculated through **.OP** command. We can then repeat the DC analysis with the following element statement.

Vd 101 0 DC -215.17μv

So the input bias current can be calculated as

I_B = 0nA

- Input offset current (I_{io})

The input offset current can be calculated with the help of difference of two currents. Since here input bias current is 0 nA so input offset current is also 0 nA.

I_{io}= 0nA

- Power dissipation (P_d)

The total power dissipation can be calculated by P=V×I. Here current at Power supply is from +5 volts to -5 volts that is equal to 10 volts and current at V_{ss} is 0.3935×10^{-4} so power can be calculated as:

P_d =V×I

$P_d = 10 \times 0.3935 \times 10^{-4}$ W

P_d = **0.03935×10^{-2} W**

- Slew rate (SR)

It is defined as the maximum rate of change output voltage per unit of time and is expressed in volts per millisecond. In equation form

SR= dV_o / dt maximum V / microsecond.

On the completion of the Spice simulation the waveform editor will show the following results. This is shown in figure 6.

Negative-going slew rate = -2.1×10^{5} V/micro second
Positive-going slew rate = $+4.0 \times 10^{5}$ V/micro second

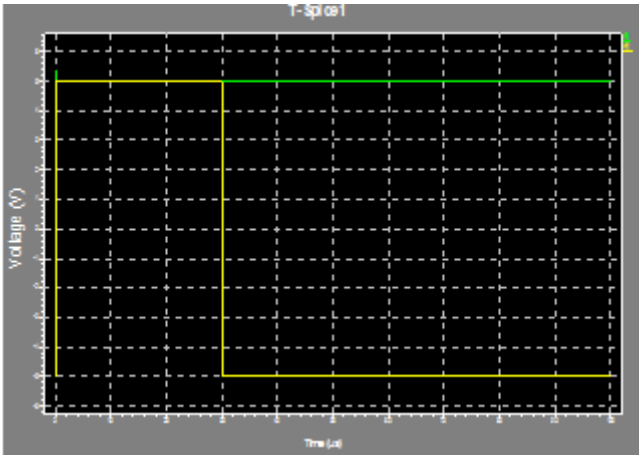

Figure 6: Slew rate waveform of CMOS op-amp circuit

5. Results of BJT and CMOS OP-AMP

A comparison of op-amp parameters of BJT (741) operational amplifier and CMOS operational amplifier is shown in table 1.

Table 1: Comparison table of different op-amp parameters of 741 BJT and CMOS Op-Amp

S. No.	*Parameters*	*BJT Op-amp*	*CMOS Op-amp*
1	Linear region	359.89 micro volts to -268.44 micro volts	9.18×10^{-4} V to $+11.9 \times 10^{-4}$ V
2	Output voltage swing	-13.28 volts to +13.18 volts.	-4.74V to +4.58V
3	DC voltage gain	2.893×10^{5}	44.213×10^{2}
4	DC offset voltage	-3.1183×10^{-4}V	-2.1517×10^{-4} volts
5	Input bias current	34.3×10^{-9}A	0nA
6	Input offset current	0.2×10^{-9}A	0nA
7	Power dissipation	5.5194×10^{-2}W	0.03935×10^{-2} W
8	Positive going slew rate	+0.544 V/micro second.	$+4.0\times10^{5}$ V/micro second
9	Negative going slew rate	-0.313 V/micro second	-2.1×10^{5} V/micro second

6. Conclusion and Future Scope

Since in this project I worked on the Op-amp using BJT and CMOS both I found that somewhere the application of BJT is good due to its some of parameters good responses like current controlling and speed but I also found that somewhere or in fact in many applications CMOS Op-amp is quite good over BJT because of its very less power consumption which is one of the most important feature as far as industries concern and for practical uses and another major feature is its slew rate which is also very fast than BJT its offsets current is also very much reduced and gain and frequency response is quite efficient and smooth over BJT. So overall CMOS OP-amp now a days going to replace most of BJT Op-amps but still due to some good characteristics of BJT's in some applications we need BJT's Op-amp. Therefore due to the importance of both the devices we switched on the new technology which is very efficient and well known now days that is BiCMOS technology. So we can further work on lots of researches in this field in which we can try to improve all the parameters further by utilizing the advantage of both the previous research results and can study further to enhance the capacity and efficiency of Operational amplifier. So it can play more important and advantageous role in electronics world.

The future implications of the project are very wide since Operational amplifier is a device which is now a day's using in many applications The project I have undertaken can be used as a reference or as a base for realizing the op-amp circuits so it can be further implemented in other projects of greater level such as reduction in power using miller capacitance technique, to reduce input bias current, to increase the slew rate etc.

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Author Profile

Ashish Kumar Singh, M.Tech student (V.L.S.I) at Gyan Vihar School of Engineering and Technology, Jaipur, Rajasthan. He has completed his B.Tech (Electronics and Communication) in 2013 under Dual Degree Program at Gyan Vihar School of Engineering and Technology, Jaipur. His main research interests are in BJT feedback amplifier.

Mrs Nidhi Goyal, is an Assistant Professor at Jagannath Gupta Institute Engineering of Technology. She has completed her M.Tech (V.L.S.I) from Suresh Gyan Vihar University in 2010 She has completed B.Tech in Electronics and Communication from Rajasthan Technical University in 2003.