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Inculcation of Simultaneous Clock Gating and Power Gating in Sequential Design

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Abstract: ***This paper presents simultaneous use of clock gating and power gating in a sequential circuit, we have taken True Single Phase Clock (TSPC) FF. Clock gating is use to reduce the dynamic power whereas power gating technique is the best way to minimize the leakage current. If both the technique use in single circuit then we can minimize the power consumption and increase the performance of the circuit which also reduce the cost of the circuit, as also cost depends on the power consumption.***

Keywords: Clock gating, Power gating, TSPC FF, Sequential circuit.

1. Introduction

As we know that VLSI is depend on the three major factors which is power, cost and speed. Power consumption is the vast issue in the present era and every new design is made to reduce the power. If power get reduce then the cost automatically get reduce and performance of the circuit increases. We are working on sequential circuits to minimize the power by applying clock gating and power gating technique in a single sequential circuit.

Clock gating technique uses a gated clock pulse which is feed in the desire circuit. We use AND gate for gated clock signal. Instead of applying clock pulse we apply pulse to the AND gate with the enable signal, when both the inputs are “high” only then the out goes “high”. Hence the gated clock gives output high only in one condition and we can reduce the dynamic power using this technique.

Power gating technique is use to reduce leakage current to some extent. In power gating we use sleep transistors, which is used to reduce the leakage current at pull down network. By applying fine-grain power gating approach, a “sleep” transistor is added to each and every cell, although the power of each cluster of cells is gated individually. Power gating is a modern technique that uses “sleep” transistors as high Vt devices to disconnect low Vt logic cells from the supply or ground to reduce the leakage in the sleep mode.

In this paper we will discuss two sections, first we will discuss about the previous work clock gating and power gating technique in section 2, and then we will discuss the proposed work under section 3 in which we will use both the technique in a sequential TSPC FF.

2. Previous Work

In previous work [1][2] we can notice that clock gating and power gating used in a single circuit, drawbacks and limitation of combining both the technique has been discussed, clock gating gives solution of circuit testability, formal verification and time closure. In power gating sleep transistor driven by the same sleep signal. This technique is best on large circuits, sleep transistors can control clusters presents in gates. The three major problem clustering, size of ST and design of circuitry has been resolved to integrate both CG and PG in a single circuit.

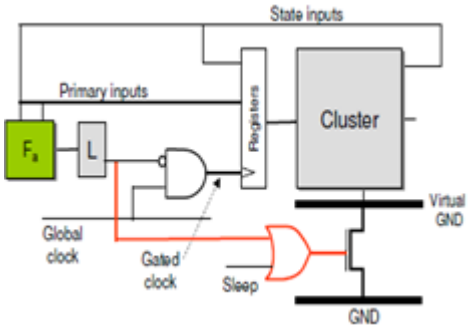

Figure 1: Integration of CG and PG

Combining CG and PG [1] is convenient when the energy necessary to reactivate the circuit is smaller than the leakage energy consumed by the circuit in the idle state. CG is done via open database. Pulse applies directly to the design and also checks the simulation of the design with CG. This is the total technique which needed to setup the design and then if above steps would be done successfully then only add sleep transistor which is PG process.

Low power design using CMOS based on T-SPICE simulator [3] in which enumerates low power. MTCMOS has been proposed which is based on DFF. As we discussed in the first paper that an extra NMOS is add in the TSPC FF which changes its functionality to low power design. As we are aware that in electronics devices Flip-Flops are the best source to stores the logical state of one or more than one data input signal. During the rise and fall signal data stored in a set of Flip-Flop present currently due to which we can feed it as an input to the other sequential circuit. Double edge triggered Flip Flops stores the data on both the edges.

3. Proposed Work

3.1) Sequential TSPC FF

Low power design TSPC FF is modify version of D FF, the circuit consists of dual TSPC FF, we can say it is a sequential TSPC FF in which the output of first is the input of the second stage. Our aim is to reduce the power

consumption (dynamic +leakage) power. D and clk is initial input for the circuit.

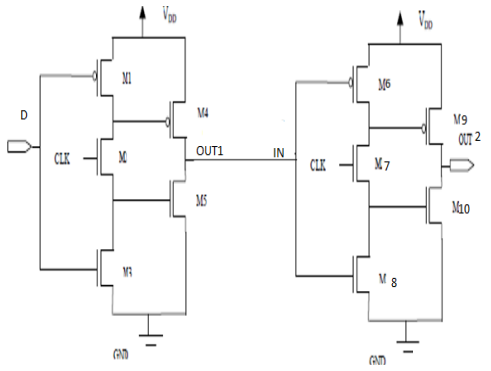

Figure 2: Sequential TSPC FF

3.2) Clock Gating

CG is AND gate with two input signal named EN and clock and the output is gated clock which is input clock pulse to reg_A instead of "clock".

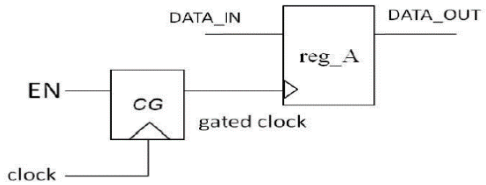

Figure 3: Clock Gating

When both En and clock are "1" then gated clock is "1". Hence dynamic power get reduce.

3.3) Power Gating

An additional sleep transistor is added to the pull up or to the pull down network. Larger sized devices are useful only when interconnect dominated. Minimum sized devices are usually optimal for low-power. Glitches causes spurious transitions, gates have nonzero delay, Glitches due to mismatch in path lengths of circuit.

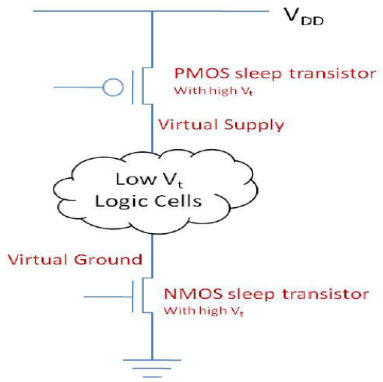

Figure 4: Power Gating

Glitches can be eliminated using insertion of buffers to equalise gates path lengths or we can redesign the circuit.

3.4) Sequential circuit with CG and PG

We use CG and PG in TSPC FF and then compare it from the circuit without CG and PG technique. It is a dual or sequential design of TSPC FF, in which AND gate is use to provide gated clock signal as an input clock of the stage 1 TSPC and the second AND gate provides the gated clock pulse to the second stage TSPC FF.

TSPC FF consists of 5 transistors, the 3 additional pull down circuitry use to minimize the leakage power. 2.5V voltage source is provided to the circuitry. We use back end tool to simulate the design. The wave form shows power and voltage of each stage.

The proposed circuit consists of 28 transistors, initially we provide Clk and D as an input in AND gate, then the output of AND gate which is Clk1 become one of the input to the stage 1 TSPC with D. Clk1 works as a gated clock. After that output of stage 1 which is Out1 fed as one of the input of second AND gate and the second AND gate, which generate Clk2 as an output. Clk2 is fed as one of the input to the second stage TSPC FF.

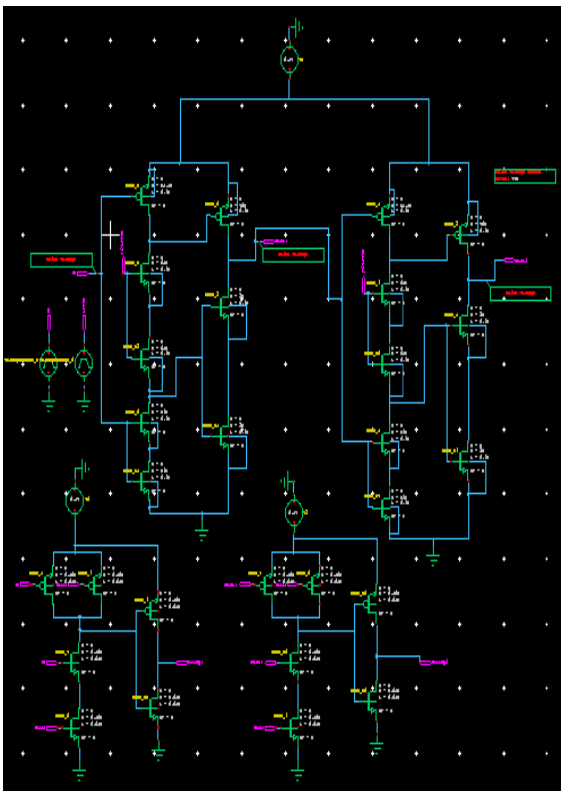

Figure 5: Schematic diagram of Sequential TSPC FF with CG and PG

Hence by applying clock gating technique in both the stage we can minimize dynamic power. Now the additional 3 transistors used in pull down network remove or eliminates the glitch or minimize the leakage to some extent and resolve the issue of leakage power. Which technique minimizes power consumption up to 20-30%.

4. Result and Comparison

In this paper we used CG and PG technique in a sequential circuit, if we did not use this technique than it is not possible to reduce the power consumption to that level.

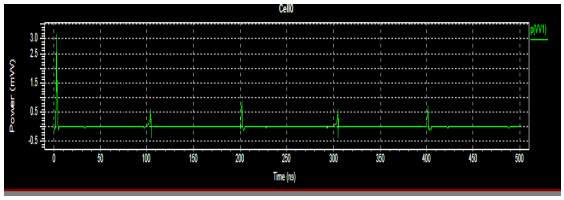

Figure 6: Power waveform of sequential circuit when apply CG and PG.

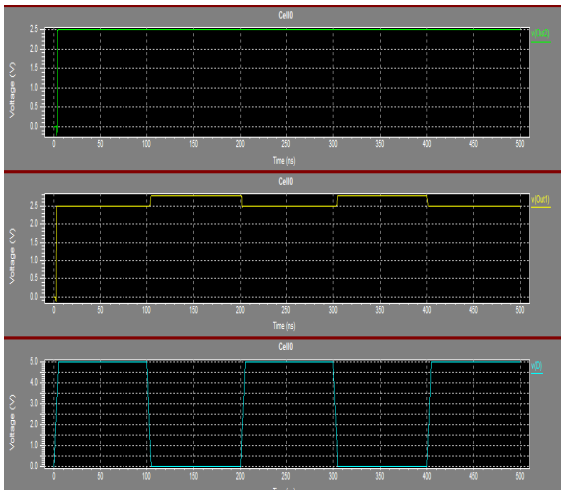

Figure 7: Voltage waveform of sequential circuit when apply CG and PD

Here we took 2.5 voltage source and the power difference between the conventional and proposed design is 7.59345e-001 mW.The delay time also reduced by 0.32 sec.

Table 1: Comparison table

Design	Power (mW)	Time(s)
Sequential TSPC FF	2.34282e-005	2.47
Sequential TSPC FF with CG and PG	9.93627e-006	2.15

5. Conclusion and Future Scope

In this paper, True Single Phase Clock (TSPC) based on logic DFF is implemented using automatic clock gating and power gating simultaneously. This method could apply on combinational or sequential circuits. Proposed work is for minimizing the power consumption and delay timing so that it is better to use the module in future those can work on less power. This can reduce cost. In gating we used cell which also consumes power and some time.

We will observe that “42.41%” of power get reduced, we can reduce the time up to “74.4%”. Combining CG and PG is convenient when the energy necessary to reactivate the circuit is smaller than the leakage energy consumed by the circuit in the idle state. We can implement the circuit by using other tool like Xlinix and Cadex, and it is also possible to reduce delay time by reducing the number of transistors, our work also get implement by reducing the size of the wire used in then circuit.

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