core via certain router it has to check whether it is operating correctly for that purpose a router has to check initially that the router is the current operator and weather the previous router obeys the XY algorithm, if it obeys the algorithm then the router conformed that the router has no error or else further it checks the availability of the router in the path by checking the diagonal availability indication. On checking that availability link if the router in the path is unavailable then checks weather the input for this router is for bypass operation if not it says the router has an error or else it confirmed that the router has no error.

3. Results and Performance Evaluation

A. Simulation Results and Performance Evaluations

The designed NoC architectures are simulated and the required parameters are calculated using the tool ModelSim, which is used as a simulation and debugging tool for VHDL, verilog and mixed language designs and the tool Quartus, which is used to synthesis the network designed using VHDL Hardware description language[2], [6]–[9].

In this designed reliable NoC the message takes an alternative path to reach the destination if there is any fault in the path through which it has to transmit the message, thus the message reach the destination even the router in the transmitting path is faulty. The simulation output for both non faulty networks is shown in Fig.4

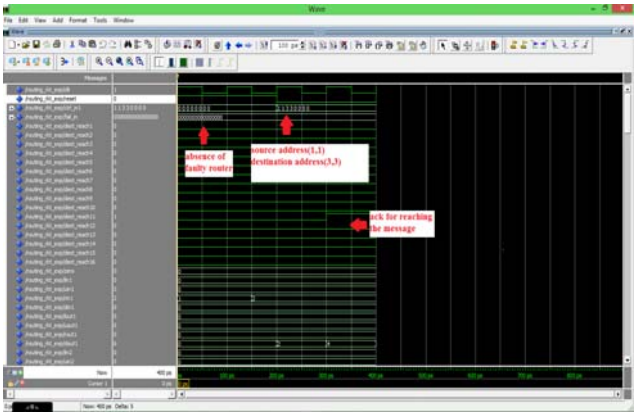

Figure 4: Simulation without any fault

The main advantage in this designed router is that the message can reach the destination even there is fault in the path through which the message travels and the simulation output for a network with faulty node is given in Figure 5.

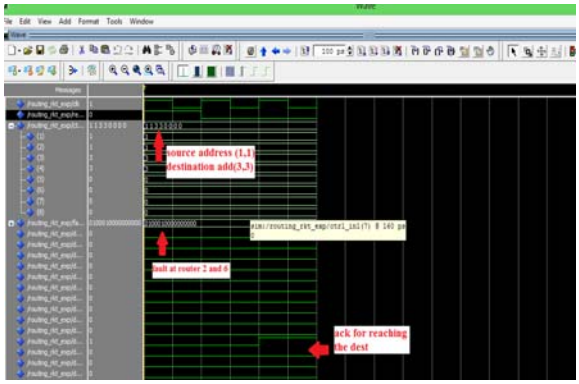

Figure 5: Simulation with faulty node

The RTL schematic for the designed RKT-NoC is given in Fig.6 which is a 4 × 4 2d mesh network.

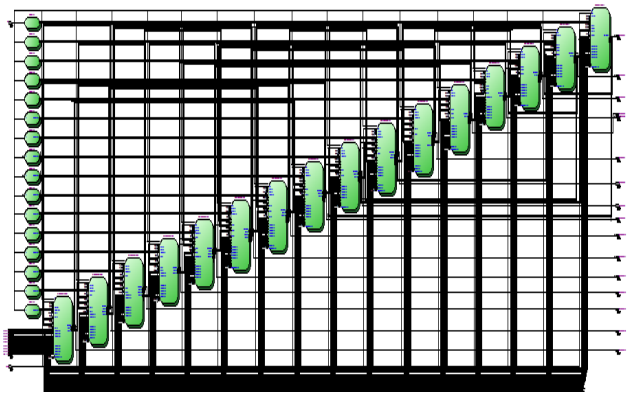

Figure 6: RTL schematic for RKT-NoC

B. Synthesis Results And Performance Evaluations

FPGA Synthesis Results:The results presented are obtained considering RKT switches configured to process data packets of four flits and able to hold two data packets in each input buffer. Table III shows the synthesis results of 4 × **4** RKT-Switch synthesis results using cyclone- II that are slices ,registers, delay(tco), FIR frequency (Mhz) and power for different sizes of data bus and FPGA technologies (Cyclone-II Quatrus FPGA).

Table I: 4 × 4 Rkt-Switch Synthesis Results Using Cyclone- II

Databus width (bits)	Slices	Registers	Delay(tco) Ns	FIR Frequency (Mhz)	Power(Mw)
4	48	16	7.159	380.08	73.67
8	59	16	7.837	380.08	74.77
16	61	16	7.963	380.08	76.01
24	61	16	7.963	380.08	76.01
32	60	16	7.658	380.08	77.05
64	60	16	7.587	380.08	78.17
128	62	16	7.773	380.08	79.30
256	65	16	8.631	380.08	80.18

It can be seen that for **4×4** the 64-b RKT-switch requires 223 registers and 959 LUTs and can operate up to 217.34 MHz on the Cyclone-II FPGA technology. We have also synthesized RKT-NoC for several sizes on the Quartus Cyclone-II technology. These results are given in Table III. The synthesis results clearly show that our architecture can be efficiently implemented in FPGA technology. It can be stated that an attractive trade-off between high speed and logic resources has been achieved.

In this paper we calculated latency, throughput. For a 2 × 2 RKT-NoC, the maximum average latency is 14 and throughput of 2 ×2, 3×3 and 4 ×4 are 2650.8, 5404.2 and 1803.7 for data bus width of 256. The maximum frequency Rate is 380.08the equations for latency and throughput are

$Latency_{RTRmin}=N_{flit}+Latency_{ECC}+3$
$Throughput_{max}=N_{IP} * n * FIR_{max} * f$

Table II: Throughput Evaluation for RKT-NoC Size of 2 × 2, 3 × 3 and 4 ×4

	RKT-NoC Size		
	2 × 2	3× 3	4 × 4
Data bus width (bits)	Throughput	Throughput	Throughput
4	42.4	101.9	34.0
8	88.7	212.8	62.1
16	172.7	370.9	122.2
24	287.5	596.2	183.3
32	361.9	881.8	224.1
64	695.6	1533.9	513.0
128	1286.5	2691.2	1001.4

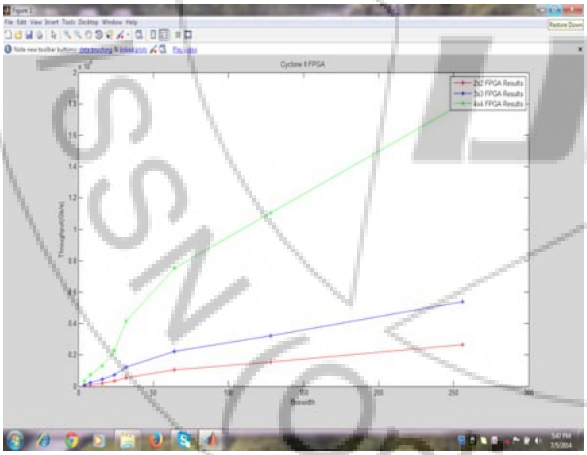

Figure 7: Throughput of one RKT-switch for different data widths

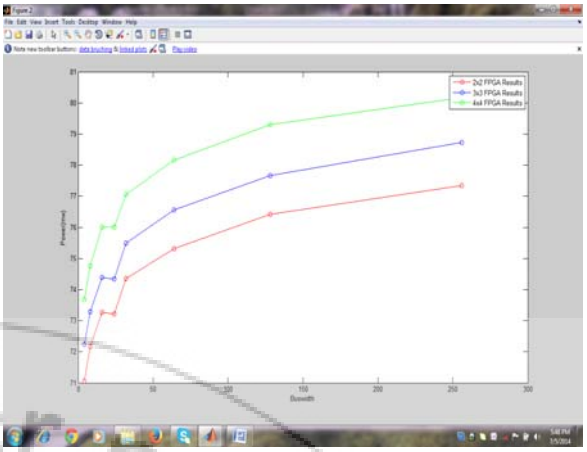

Figure 8: Power of one RKT-switch for different data widths

4. Conclusion

The RKT-NoC is highly reliable when compared with ordinary NoC due to the addition of error detection mechanism in the design and it avoids the dead lock and live lock problem. Hence it shows better performance in operation and due to the presence of error correcting code the repeated usage of the logic elements reduces and hereby it is clear that the designed RKT-NoC is more advantageous than the ordinary NoC.

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