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Design & Analysis of Modified Conditional Data Mapping Flip-Flop to Ultra Low Power and High Speed Applications

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Abstract: ***In the history, the major issues of the VLSI designer were area, cost, performance, and reliability; power concern was typically of only lesser importance. But more than the last few years' power in the circuit is the major difficulty at the present days which is being faced by the very large scale integration industries. The power dissipation in several circuits is typically take place by the clocking system which includes the clock distribution system and sequential elements (flip flops and latches) in it. The quantity of power dissipation by any clock distribution system and sequential circuit in any chip is as regards of 30% to 60% of the overall chip power dissipation by the circuit. Clock is the most vital signal present in the chip. Clock signals are synchronizing signals which offer timing references for computation of in the least work in synchronous digital systems. In this paper the power of the sequential circuit is reduced which in position reduce the on the whole power of the chip. Here dissimilar low power techniques for the lowering static power dissipation are second-hand in the sequential circuit are surveyed. The work analyses the power consumption and propagation delay of flip- flop designs. In Tanner 14.0µm CMOS technology designs are implemented.***

Keyword: Flip-flop, Low power, CMOS Circuit, delay optimization.

1. Introduction

In the past, the major concerns of the VLSI designer were area, performance, cost and reliability. Power consideration was mostly of only secondary importance. In recent years, however, this has begun to change and, increasingly, power is being given comparable weight to area and speed considerations. One of the important factors is that excessive power

Consumption is becoming the limiting factor in integrating more transistors on a single chip or on a multiple-chip module. Power consumption is dramatically reduced; the resulting heat will limit the feasible packing and performance of VLSI circuits and systems. Most of the current designs are synchronous which implies that flip-flops and latches are involved in one way or another in the data and control paths. One of the challenges of low power methodologies for synchronous systems is the power consumption of the flip-flops and latches.

Flip-Flops and latches are the basic elements for storing information. One latch or Flip-Flop can store one bit of information. The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately when their input change. Flip-flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even. There are basically four main types of latches and flip-flops: SR, D, JK, and T. For each type, there are also different variations that enhance their operations. Figure 1(a), (b) illustrates the difference between positive edge triggered flip flop and an active high latch. At the same time as it can be seen in this figure, likely changes of input can be seen at the output of the latch as it is transparent.

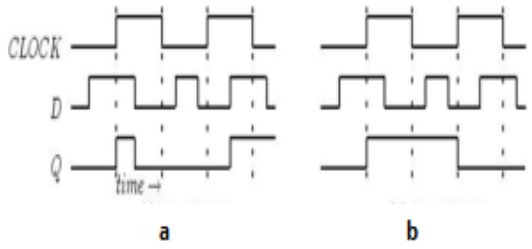

Figure 1: (a) Active High latch **(b)** Positive Edge Triggered Flip-Flop

The presentation of a flip-flop is calculated by three main timings and delays: propagation delay (Clock-to-Output), setup time and hold time. Setup time and hold time define the connection between the clock and input data as shown in the Figure 1(c). Setup time and hold time explain the timing necessities on the D input of a Flip-Flop with admiration to the Clk input. Setup and hold time describe a window of time which the D input have to be valid and stable in order to guarantee valid data on the Q output. Setup Time (Tsu) Setup time is the time that the D input must be valid before the Flip-Flop samples. Hold Time (Th**)** – Hold time is the time that D input must be maintained suitable after the Flip-Flop samples. Propagation Delay (Tpd) – Propagation delay is the time that takes to the sampled D input to propagate to the Q productivity.

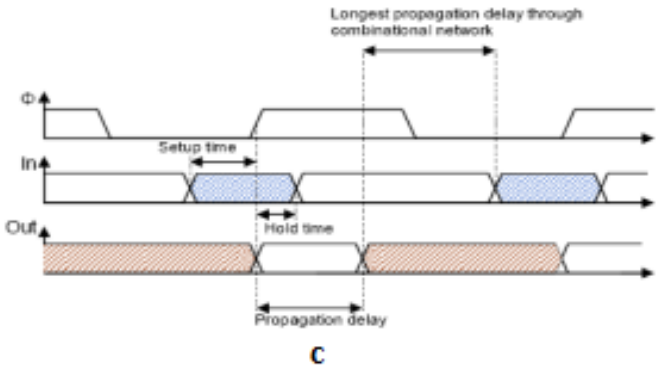

Figure 1: (c) Timing Diagram

There is a broad collection of flip-flops in the journalism [1]. Many modern microprocessors selectively employ master-slave and pulsed-triggered flip-flops [2]. Conventional master-slave single-edge flip-flops, for illustration, transmission gated flip-flop [3], are completed up of two stages, one master and one slave. One more edge-triggered flip-flop is the sense amplifier-based flip-flop (SAFF) [4]. Every one of these hard edged-flip-flops is characterized by means of a positive setup time; cause large D-to-Q delays. On the other hand, pulse-triggered flip-flops reduce the two stages into one stage and are characterized by the soft edge possessions. 95% of all static timing latching on the Itanium 2 processor employs pulsed clocking [5]. Pulse triggered flip-flops might be classify into two types, implicit-pulsed and explicit-pulsed, for illustration, the implicit pulse-triggered data-close-to-output flip-flops (ip-DCO) [6] and the explicit pulse-triggered data-close-to-output flip-flops (ep-DCO) [6]. The relationship between Conventional Conditional Data Mapping Flip-flop and Clock Pair Shared D flip flop (CPSFF) here we are examination the working of CDMFF and the conventional D Flip-flop [7]. CDMFFs for low-power and high-performance flip-flops, namely conditional data mapping flip-flops (CDMFFs), which reduce their dynamic power by mapping their inputs to a arrangement that eliminates redundant internal transitions. We nearby two CDMFFs, having differential and single-ended structures, correspondingly, and contrast them to the state-of-the-art flip-flops. It is vital to save power in these flip-flops and latches with no compromising state integrity or performance [8]. High speed parallel counter is scheming to get high operating frequency and to reduce the power consumption, and it can be achieved from side to side a novel pipeline portioning technology [9]. The contrast between Conventional Conditional Data Mapping Flip-flop and Clock Pair Shared D flip flop (CPSFF) here we are checking the working of CDMFF and the conventional D Flip-flop.

Due to the immense growth in nanometer technology [10], A low power pulse triggered Flip-flop (P-FF) design is done by the pulse generation control logic, an AND function, is uninvolved from the critical path to facilitate a faster discharge operation. A conditional pulse enhancement technique is devised to speed up the discharge the length of the critical path only when needed [11].

2. Surveyed Low Power Flip Flop Design Techniques

Power consumption is depends on more than a few factors, the total power is sum of dynamic, short circuit and leakage power dissipation. Dynamic power indulgence is function of frequency, supply voltage, data activity. Based on these factors, there are a variety of ways to lower the power consumption shown as follows.

1) Double Edge Triggering: By means of half frequency on the clock distribution network will save just about half of the power consumption on the clock distribution network. On the other hand the flip-flop must be able to be double clock edge triggered.

For example, the clock division shared implicit pulsed flip-flop (CBS-ip DEFF), is a double edge triggered flip-flop. Double clock edge triggering technique reduces the power by falling frequency f in equation.

2) Using a low swing voltage: on top of the clock distribution network can diminish the clocking power consumption since power is a quadratic function of voltage. To use low swing clock sharing, the flip-flop should be a low swing flip- flop.

For example, low swing double-edge flip-flop (LSDFF) is a low swing flip-flop. In adding up, the level converter flip-flop is a natural applicant to be used in low swing atmosphere too. For example, CD-LCFF-ip might be used as a low swing flip-flop since received signals only make nMOS transistors. The low swing technique reduces the power utilization by declining voltage in equation.

3) There are two ways to reduce the switching activity: Conditional operation (do away with redundant data switching: conditional discharge flip-flop (CDFF)), conditional capture flip-flop (CCFF) or clock gating.

a) Conditional Operation: For dynamic flip-flops, similar to hybrid latch flip-flop (HLFF), semi dynamic flip-flop (SDFF), here are redundant switching activities in the internal node. When input stay at logic one, the internal node is reserved charging and discharging without the stage any useful calculation. The conditional operation method is needed to control the redundant switching.

For example, in CDFF, a feedback transistor is inserted on the discharging path of 1st stage which will revolve off the discharging path when D keeps 1. Internal node will not be set aside discharging at every clock cycle. In CCFF, It neither uses a clocked NOR gate to control an nMOS transistor in discharging path when Q keeps 1. The superfluous switching activity is detached in both cases. This reduces the power utilization by decreasing data activity.

b) Clock Gating: At what time a certain block is inactive, we can put out of action the clock signal to that block to save power. Gated master slave flip-flop is used. Both conditional operation and clock gating methods decrease power by decreasing switching activity.

4) Using Dual Vt/MTCMOS: To decrease the leakage power in standby mode. With scaling feature size, the leakage current increases rapidly, the MTCMOS technique as well as transistor stacking, dynamic body biasing, and supply voltage ramping could be used to reduce leakage standby power consumption.

5) Reducing Short Current Power: Divide path can reduce the short current power, because pMOS and nMOS are driven by separate signals.

6) Reducing Capacity of Clock Load: 80% of non-clocked nodes have switching activity less than 0.1. This means reducing power of clocked nodes is vital because clocked node has 100% activity. One useful way of low power design for clocking system is to reduce clock capacity load by minimize number of clocked transistor. Several local clock load reduction will also decrease the global power consumption. This technique reduces power by decreasing clock capacity.

3. Surveyed Techniques for Reducing Switching Activity

A large part of the on-chip power is consumed by the clock drivers. For example, CCFF used 14 clocked transistors, and CDFF used 15 clocked transistors. In difference, conditional data mapping flip-flop (CDMFF, Fig. 2) used only seven clocked transistors, resulting in about 50% reduction in the number of clocked transistors, hence CDMFF used less power than CCFF and CDFF. (Note that CDFF used double edge clocking. For simplicity purpose, we did not include the power investments by double edge triggering on the clock distribution network). This shows the value of reducing clocked transistor numbers to achieve low power. Since CDMFF outperforms CCFF and CDFF in view of power consumption, we do not talk about CCFF or CDFF further in this paper.

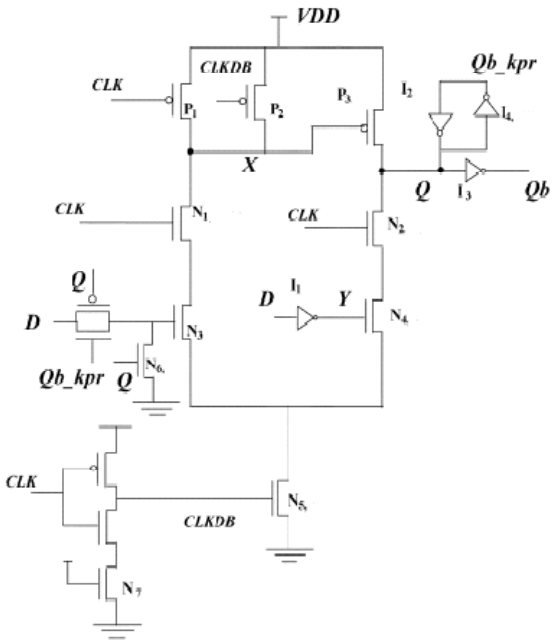

Figure 2: CDMFF

On the other hand, there is redundant clocking capacitance in CDMFF. When data remains 0 or 1, the precharging transistors, P1 and P2, keep switching not including valuable computation, resulting in redundant clocking. Obviously, it is necessary to reduce redundant power consumption here. Further, CDMFF has a floating node on critical path for the reason that its first stage is dynamic. When clock signal CLK transits from 0 to1, CLKDB will stay 1 for a short whereas which produces an implicit pulse window for evaluation. For the period of that window, both P1, P2 are off. In addition, if D transits from 0 to 1, the pull down network will be detached by N3 using data mapping method (N6 turns off N3); If D is 0, the pull down network is detached from GND as well. Hence internal node X is not connected with Vdd or GND during most pulse windows, it is basically floating periodically. With characteristic size shrinking, dynamic node is more flat to noise interruption since of the undriven dynamic node. If a close by noise discharges the node X, pMOS transistor P3 will be partially on, and a glitch will appear on output node Q. In a nanoscale circuit, a glitch not simply consumes power but could propagate to the after that stage which makes the system more susceptible to noise. Hence, CDMFF could not be used in noise concentrated environment. Unlike CDMFF, other dynamic flip-flops employ structure to prevent the floating point. For example, SDFF has a keeper at node X while HLFF, and CCFF have a transistor connecting to Vdd when D=0, correspondingly. Both methods give out to increase noise toughness of node X.

Lastly it is not easy to apply the low power techniques introduced in earlier section to CDMFF. For example, the clock structure with precharging transistors P1, P2 in CDMFF (Fig. 2) makes it difficult to apply double edge triggering. Nor can CDMFF be used in low swing clock surroundings. (Note that the established low swing clock signal cannot drive pMOS, P1 and P2, in high voltage block (VDDH), since the pMOS transistors will not turn off by a low swing voltage, resultant in short circuit power consumption.)

4. Simulation Results

As shown in the fig. 3,4,5,6, The simulation results for the flip-flop were obtain in a 0.18µm CMOS technology at room temperature by TSPICE, the deliver voltage was 1.8 V. (Shown in fig 3), The parasitic capacitances are extracted from the layouts. In order to obtain accurate results, we have replicated the circuits in actual surroundings, anywhere the flip-flop inputs (clock, data) are determined by the input buffers, and the output is requisite to drive an output load. Assuming uniform data distribution, we have supplied input with 16-cycle pseudorandom input data with an activity factor of 18.75% to reflect the average power consumption. A clock frequency of 250 MHz is used.

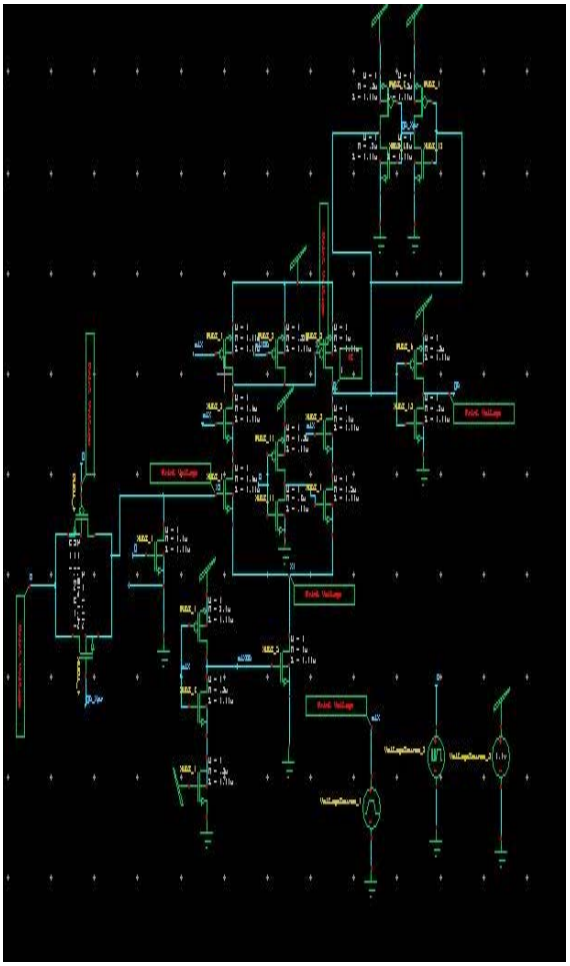

Figure 3: TSPICE capture of CDMFF

From (fig 4), Inputs are driven by the inverters, and the output is driving a capacity load of 14 minimum inverters. Each design is simulated using the circuit at the layout level. All capacitances were extracted from layout such that we can simulate the circuit more accurately. This is because the internal gate capacitance, parasitic capacitance, and wiring capacitance affect the power consumption heavily in deep sub micrometer technology. Further the delay strongly depends on these capacitors. Circuits were optimized for power delay product (PDP). Delay is data to output delay (D-to-Q delay) which is the sum of the setup time and the clock to the output delay.

Power consumed in the data and clock drivers are calculated in our reproduction. During this method, the load see by forceful logic compulsory by the flip-flop is incorporated in whole power using up. The clock influence is the power addicted by the clocked transistors. It is a very important parameter since it determines potential power saving in the clock distribution system by dropping the clock load.

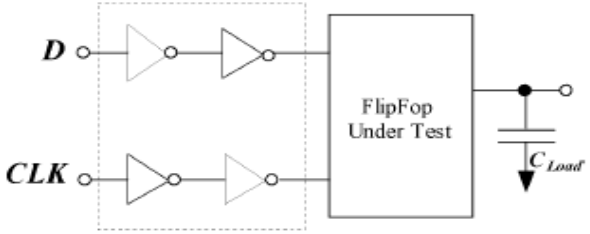

Figure 4: Setup used for simulation

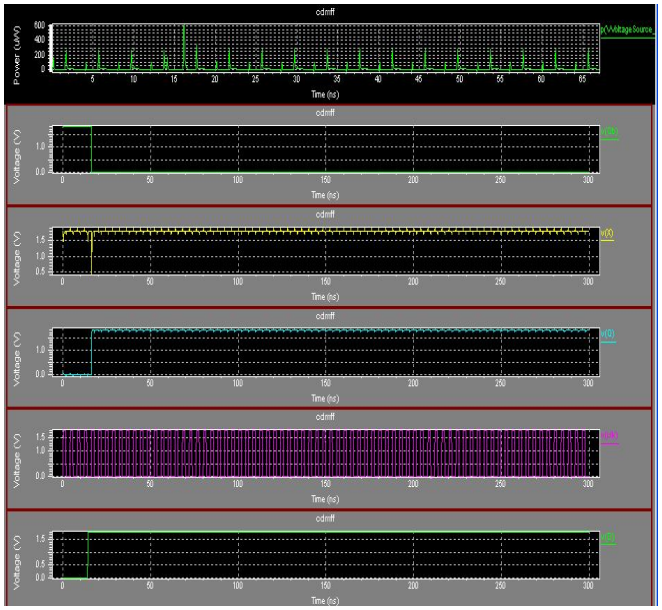

Figure 5: Waveform for CDMFF

(Fig 5, 6) shows, the waveform of CDMFF and Waveform for Power Consumption at process. CDMFF suffers from the occasionally floating point difficulty if it is in noise sensitive surroundings. Clocked pair shared scheme resolves this issue successfully. The power enhancement of CPSFF over CDMFF is larger when the switching activity is lesser.

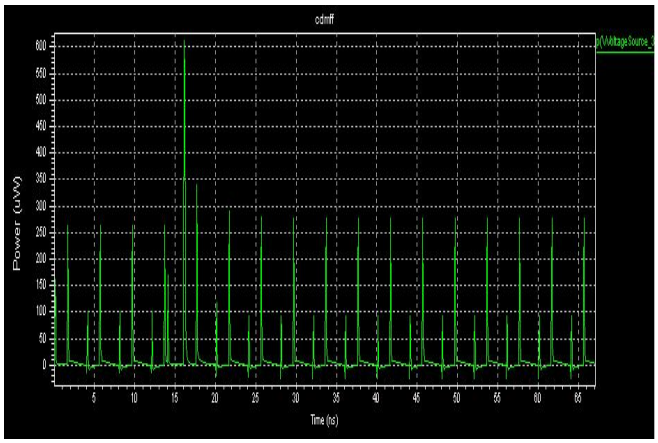

Figure 6: Waveform for Power Consumption at process

5. Conclusion and Future Scope

We bring to a close this paper by exactness an significant set of guiding principle which are the curve stone for low power flip-flop drawing methodology and low power flip-flop simulation .In general, low power design for combinational and sequential circuits is an main field and gaining more significance as time goes by and will continue an vital area of investigate for a long time. We have accessible a survey and evaluation of low-power flip-flop circuits. Our new results enabled us to recognize the power and show trade-offs of the flip-flop design.

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