ARM Advanced High-Performance Bus Complaint Inter Integrated Circuit

Prabhakar. K [1], Gowda. R. M. C.[2]

[1]Assistant Professor, Department of ECE, BITM , Bellary-583104, Karnataka, India

[2] PG Student of Digital Electronics, Department of ECE, BITM , Bellary-583104, Karnataka, India

the two different bus-architecture, wrapper can be designed as a bridge, then verify the data transfer between each other.

4. Block diagram of the Module

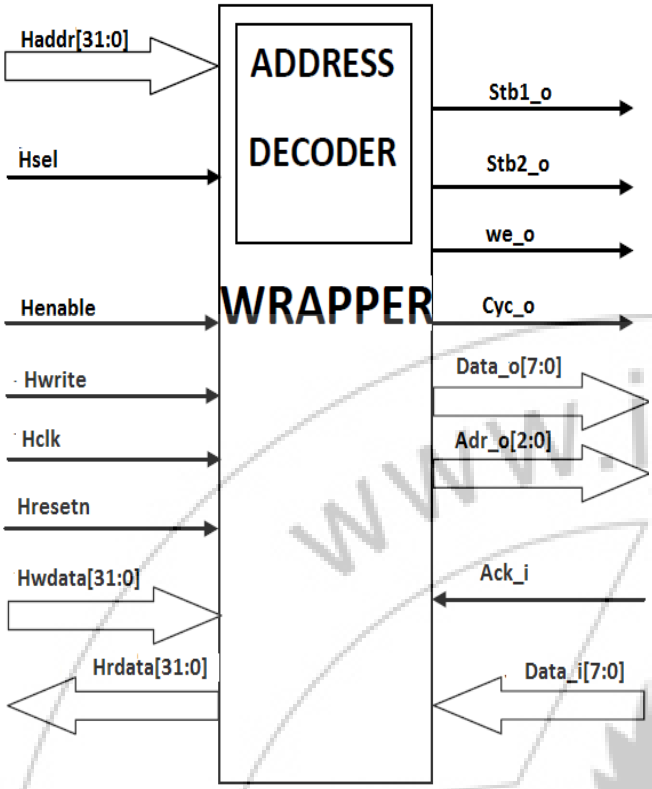


Figure 2: Block diagram of the wrapper.

The wrapper has the following functions

- Address decoding to select a particular master.
- It acts as a bridge between the AHB and I2C, as these two buses are functionally different, thereby ensuring error free data transfer between the two buses.

The I2C-Wishbone Master IP Core is used for connecting the slaves to the masters. The WISHBONE Bus interface is a free, open-source standard that is gaining popularity in digital systems that require usage of IP cores. This bus interface encourages IP reuse by defining a common interface among IP cores. That in turn provides portability for the system, speeds up time to market, and reduces cost for the end products.

6. Wrapper Logic

The working of the wrapper is as follows:

- First, depending on the value of two particular bits in the haddr, the wrapper generates the strobe signal for selecting the master and each master has its own strobe signal.
- In accordance with the control signals on the AHB and Wishbone, the operation can be classified into the read and write cycles.
- In the write cycle, the wrapper writes data onto the wishbone. A special signal present on the wishbone aids in transfers, the acknowledgement or ack signal. When the address is sent to the wishbone and it responds with an ack, only then will the apb send the data to the wishbone and from there to the respective I2C master.

In the read cycle, the wrapper reads the data from the I2C master. For this we use the flopped version of ack. This is done so because, it is observed that there is a delay of one clock cycle by the time ack is detected and the master responds with the data.

7. Wishbone-I2C-Master-Core Architecture

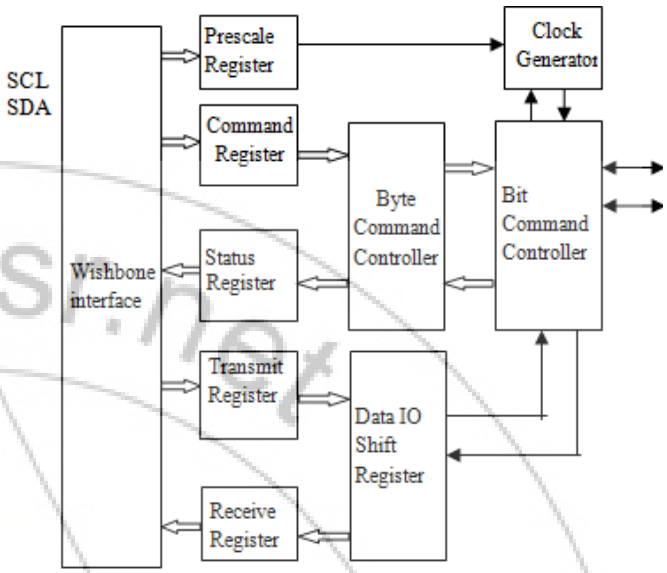


Figure 3: Block diagram of Wishbone I2C-Master core Architecture

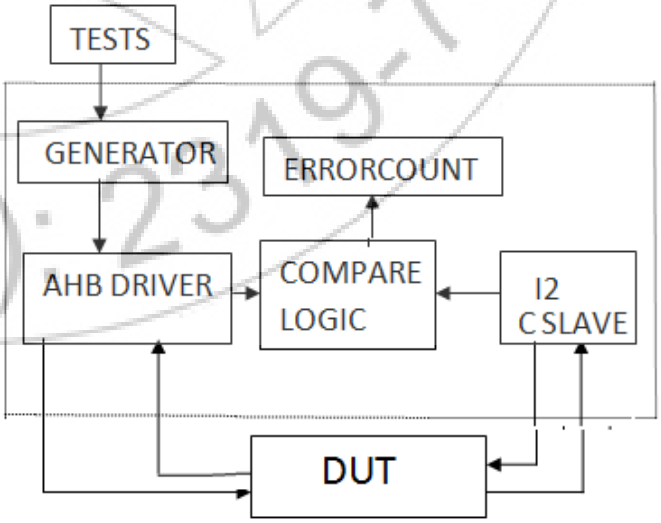
The I2C core is built around four primary blocks are shows figure3, the Clock Generator, the ByteCommand Controller, the Bit Command Controller and the DataIO Shift Register.All other blocks are used for interfacing or for storing temporary values [3].

8. Verification

Verification environment consists of following stages

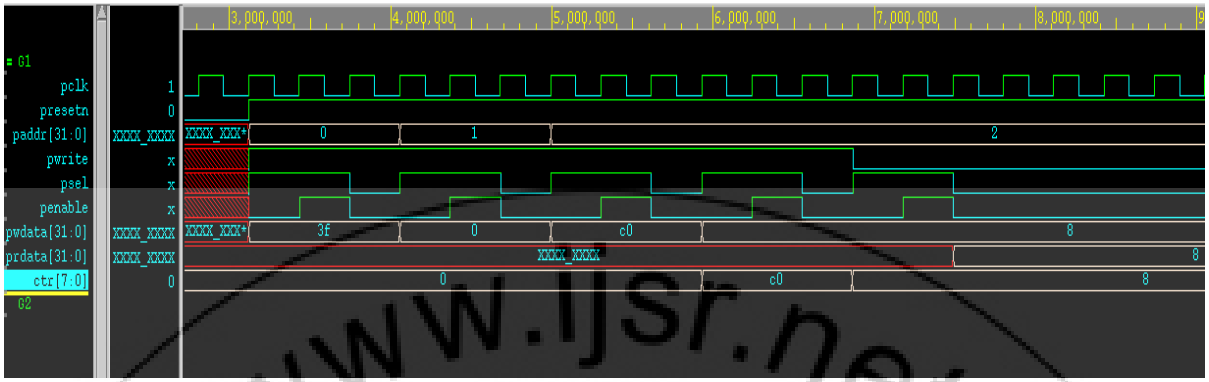
- Planning
- Feature Extraction from design specification.
- Listing out Test cases.
- Verification Environment Architecture plan.

8.1 Verification Environment Plan

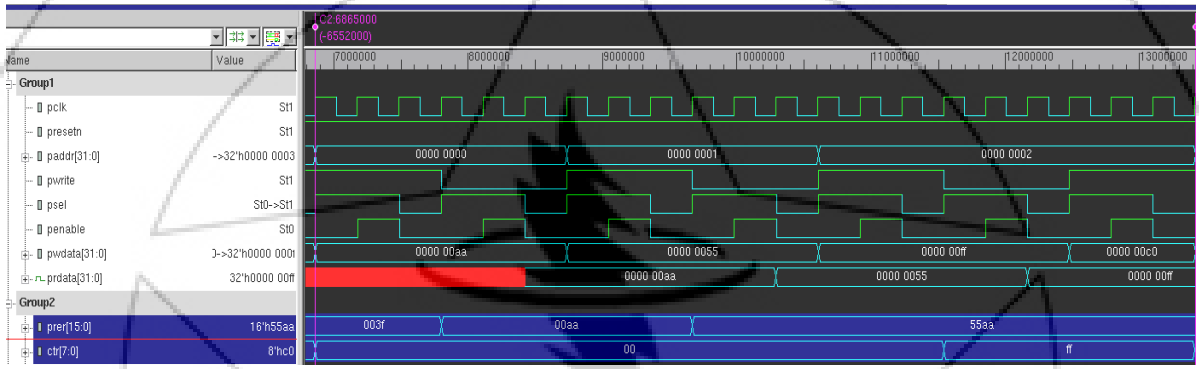


9. Results

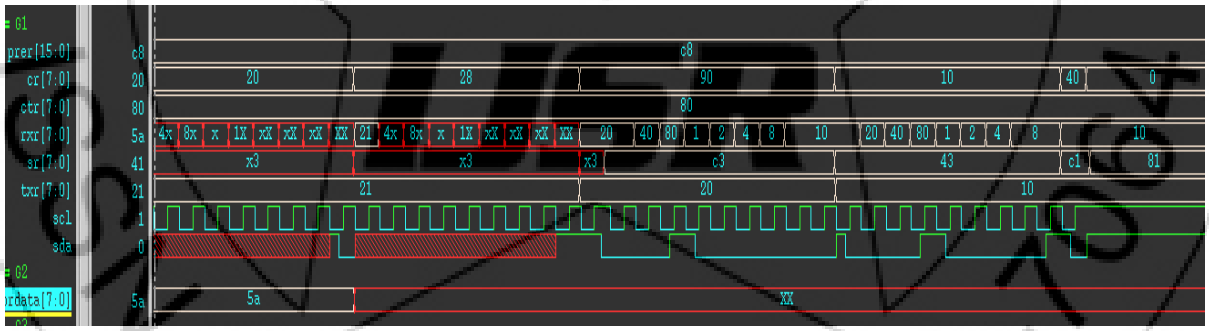
9.1 Simulation of Simple case



9.2 Simulation of register case

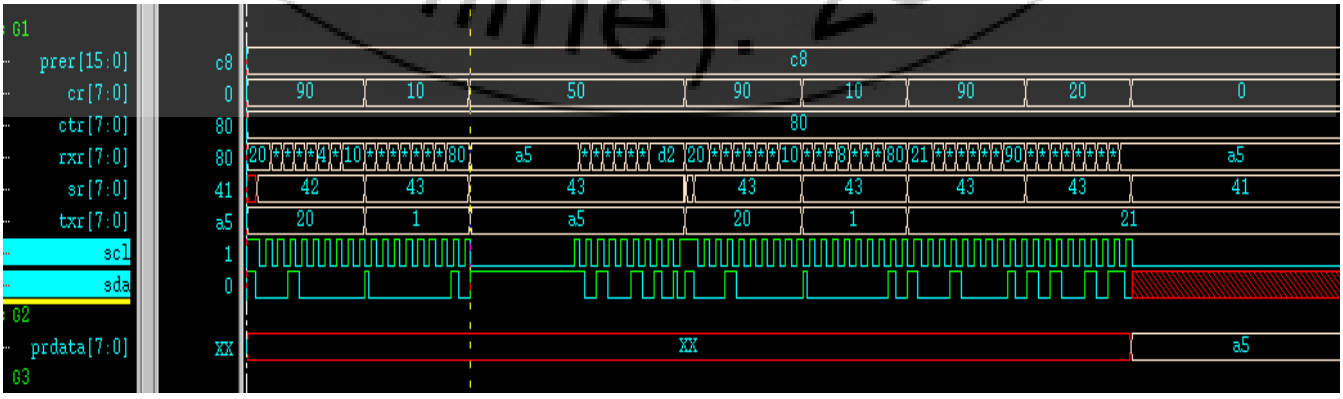


9.3 Simulation of multi test



9.4 Simulation of I2C read, write test

In this case we will verify the Wrapper and Wishbone I2C Master-Core by writing data to and reading data from slave, One byte of data is written from the AHB to the I2C slave through the DUT.



10. Conclusion and Future Scope

10.1 Conclusion

In conclusion, data transfers between two bus architectures of completely different characteristics can be achieved by a software wrapper and a supporting core. Here this core is the I2C wishbone master core. Both the design and verification phases have been successfully simulated. The test cases did cover all the corner cases of the design.

10.2 Future Scope

A few improvements which can be implemented in the current design in the future are listed below.

1. In this method only 7 bit addressing format is used. We can make it to operate in 10 bit addressing format.
2. We can make clock generator to work in different modes such as standard mode, fast mode, and high- speed mode.

References

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Author Profile

Mr. Prabhakar. K Assistant Professor, Dept of ECE, Ballari Institute of Technology & Management, Bellary-583104, Karnataka, India

Mr. Gowda. R.M.C. has completed B.E in Instrumentation Technology from Vijaya Nagar Engineering College, Bellary and Now Pursuing M.Tech in Digital Electronics from Ballari Institute of Technology & Management , Bellary-583104, Karnataka, India