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High Speed Implementation of Lifting Based Discrete Wavelet Transform (DWT) on FPGA

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Abstract: ***The objective of this project is to implement the high speed lifting-based two dimensional discrete wavelet transform (2D-DWT) algorithm on Field Programmable Gate Array (FPGA). The proposed method is based on new and fast lifting scheme with fully pipelined approach .Pipelining structure in DWT reduces hardware complexity and memory accesses and speeds up the performance. The conversion of raw image into Hex format is done using MATLAB and the Hex image is loaded into the FPGA kit. The result of the 2D-DWT provides four filtered images and is passed to display. The algorithm has been realized in Verilog HDL and implemented using XC6SLX16-CSG324C Xilinx Spartan-6 FPGA device. The currently available methods for calculating discrete wavelet transform (DWT) which is considered as conventional method of DWT requires lots of hardware (adders and multipliers).Such an implementation demands both a large number of computation and a large storage features that are not desirable for either high speed or low power image processing applications, so there is a need for calculating DWT in less amount of time with hardware minimization. Pipelined Lifting-Based DWT is one of such technique which is used to calculate DWT in fewer amounts of time and reduced hardware. The Lifting based DWT has wide areas of applications, among which medical imaging is most popular. It is used in image compression standards like JPEG, MPEG etc.***

Keywords: Discrete wavelet transform (DWT), Lifting Scheme, multi-stage pipelining, FPGA

1. Introduction

Computer data compression technique is, of course, a powerful, enabling technology that plays a vital role in the information age. The various types of data like images and videos which are commonly transferred over networks have high bit traffic. The explosive growth in demand for image and video data, coupled with delivery bottlenecks is kept at compression technology. Among the available compression standards, the JPEG image format standard is widely use today. JPEG uses the Discrete Cosine Transform (DCT) as the transform, applied to 8×8 blocks of image data. The newer standard JPEG2000 is based on the Discrete Wavelet Transform (DWT). Wavelet Transform offers the multi-resolution image analysis, which appears to be well matched to the low level characteristic of the human vision. The DCT is essentially unique but WT has many possible realizations. Wavelets provides with a basis for more suitable representation of images. This is because it can represent information in different variety of scales, with local contrast changes, as well as larger scale structures and thus is a better fit for image data

The brief theory of understanding of how any discrete wavelet transform or two band sub band filtering with finite filters can be decomposed into a finite sequence of simple filtering steps, which we called lifting steps structures. This decomposition corresponds to a factorization of the polyphase matrix of the wavelet or sub band filters into elementary matrices. This factorization provides an alternative for the lattice factorization, with the advantage that it can also be used in the bi-orthogonal. A mathematical model for the computation and interpretation concept of a multi-resolution representation explained how to extract the difference of information between successive resolutions and new define wavelet representation and also gives the application of wavelet to data compression in image coding [1]. The efficient very large scale integration (VLSI) architecture, called efficient flipping structure, is proposed for the lifting-based discrete wavelet transform. It provide a variety of hardware implementations to improve and possibly minimize the critical path as well as the memory requirement of the lifting based discrete wavelet transform(DWT) by flipping conventional lifting scheme structures. The precision issues are also analyzed. By case studies of the JPEG2000 default lossy (9,7) filter, the efficiency of the proposed flipping structure is demonstrated and also provide well featured architecture for DWT filters [2]. The recent developments in VLSI architectures and algorithms for efficient implementation of lifting based Discrete Wavelet Transform (DWT). The basic principle behind the lifting based scheme is to decompose the finite impulse response (FIR) filters in wavelet transform into a finite sequence of simple filtering steps. Lifting based DWT implementations have many advantages, and have recently been proposed for the JPEG2000 standard for image compression. In this paper, provide a survey of architectures for both 1-dimensional and 2-dimensional DWT. The architectures are representative of many design styles and range from highly parallel architectures to DSP-based architectures to folded architectures. We provide a systematic derivation of these architectures along with an analysis of their hardware and timing complexities [3]. There are many advantages over the convolution-based method. For instance it is very suitable for parallelization. The two new FPGA-based parallel implementations of the DWT lifting-based scheme. In the first, the implementation uses pipelining, parallel processing and data reuse to increase the speed up of the algorithm. In second architecture, a controller is introduced to deploy dynamically a suitable number of clones according to the available hardware resources on a targeted environment. These two architectures are able to process large size incoming images

or multi-framed images in real-time. The implementation has been done on a Xilinx Virtex-5 FPGA environment. In fact, the first architecture has given an operating frequency of 289 MHz, and the second architecture demonstrated the controller's capabilities of determining the true available resources needed for a successful deployment of independent clones, over the targeted FPGA environment and processing the task in parallel [4].

Image compression is a method through which we can reduce the storage space of images, videos which will helpful to increase storage and transmission process's performance. In image compression, main criteria is laid on reducing size but also concentrate on doing it without losing quality and information of image. In this paper, two image compression techniques are simulated. The first technique is based on Discrete Cosine Transform (DCT) and the second one is based on Discrete Wavelet Transform (DWT). The results of simulation are shown and compared different quality parameters of it are by applying on various images [5], [6]. A scheme for the design of area efficient and high speed pipeline VLSI architecture for the computation of fixed point 1-D discrete wavelet transform using lifting scheme is proposed. The main focus of the scheme is to reduce the number and period of clock cycles and efficient area with little or no overhead on hardware resources. The fixed point representation requires less hardware resources compared with floating point representation. The pipelining architecture speeds up the clock rate of DWT and reduced bit precision reduces the area required for implementation. The architecture has been coded in Verilog HDL on Xilinx platform and the target FPGA device used is Virtex-II Pro family. This scheme requires the least computing time for fixed point 1-D DWT and achieves the less area for implementation, compared with other implementation. So this architecture is suitable for real time processing of DWT computation applications [7], [8]. , The dual-tree complex wavelet transform (CWT) is a relatively recent enhancement to the discrete wavelet transform (DWT), with important additional properties: It is nearly shift invariant and directionally selective in two and higher dimensions. It achieves this with a redundancy factor of only 2d for d-dimensional signals, which is substantially lower than the undecimated DWT. The multidimensional (M-D) dual-tree CWT is nonseparable but is based on a computationally efficient, separable filter bank (FB). This tutorial discusses the theory behind the dual-tree transform, shows how complex wavelets with good properties can be designed, and illustrates a range of applications in signal and image processing. We use the complex number symbol C in CWT toavoid confusion with the often-used acronym CWT for the (different) continuous wavelet transform [9]. the application of complex discrete wavelet transform (CDWT) which has significant advantages over real wavelet transform for certain signal processing problems. CDWT is a form of discrete wavelet transform, which generates complex coefficients by using a dual tree of wavelet filters to obtain their real and imaginary parts. The paper is divided into three sections. The first section deals with the disadvantage of Discrete Wavelet Transform (DWT) and method to overcome it. The second section of the paper is devoted to the theoretical analysis of complex wavelet transform and the last section deals with its verification using the simulated images [10].

2. Lifting Based Algorithm

The Lifting scheme algorithm can be written as follows.

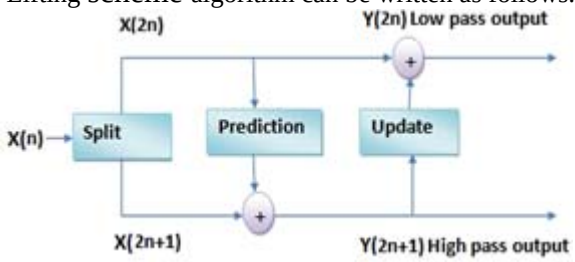

Figure 1: Split, Predict and Update Phases of the Lifting Based DWT

2.1 Split Phase

In this split phase, the original signal, X (n), is split into two subsets to separate the even samples from the odd ones.
X_e= X(2n) Even samples
Xo= X(2n+1) Odd samples (1)

2.2 Prediction Phase

At this point, the even subset X (2n) is used to predict the odd subset X (2n+1) using a prediction function P.
$Y(2n+1)= X_o(2n+1) – P(X_e)$ (2)

2.3 Update Phase

In this stage, the coefficient X (2n) is lifted with the help of the neighboring wavelet coefficients. The third step (update phase) updates the even samples using the newly calculated odd samples.
Y(2n) = Y(2n+1) + U(Xe) (3)
Where, U is the new update operator.

3. Proposed System

The Lifting-Based 2D-DWT is implemented using Verilog HDL. There are several modules implemented to achieve the functional requirement of the project, all these modules work together to produce a desired output. Following are the modules used to implement the project. The individual modules are explained below.

This module is implemented in Matlab and run on host computer. The main functionality of this block is read an original input image extract into hexadecimal format so that Verilog simulator can read the image or can be send to FPGA hardware for processing. Figure gives flow chart of the DWT block.

In this first, we will use matlab for image to hex conversion. It will generate hex file. Next in hardware block pipelined DWT operation is done and it will give Hex file. Finally, at the end using matlab we will convert hex file to image and display the result.

4. System Architecture

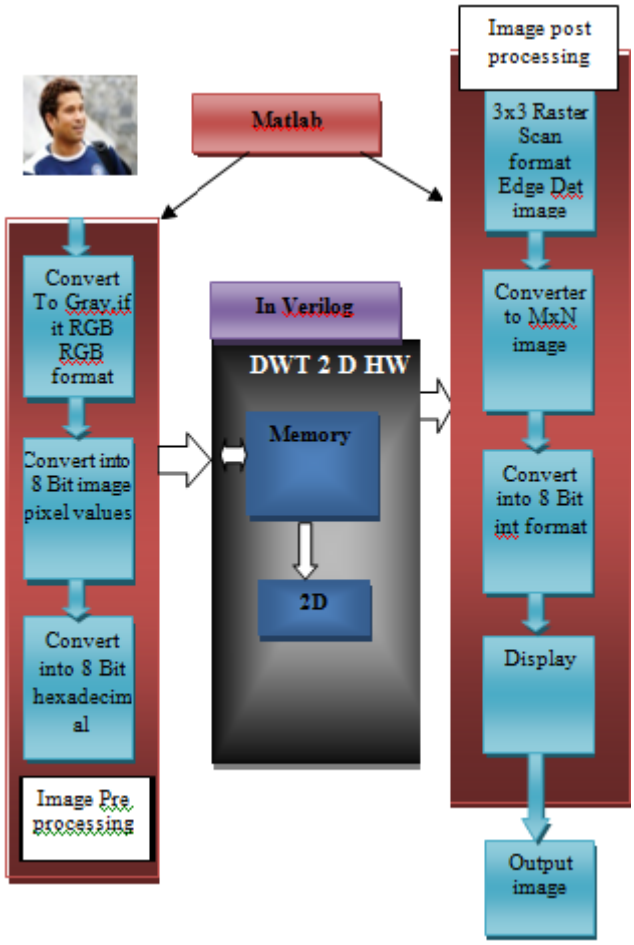

Figure 2: System Architecture

5. System Architecture description.

Above figure shows the system architecture description of the proposed project implementation. To demonstrate the work, we use matlab for pre and post processing of

- Image preprocessing block
  Image preprocessing module will be in Matlab, this block will read the RAW image of size MxN and convert into hexadecimal format, and then it will be converted to in Raster scan format with each location 24 bit (3 pixels in a Row). Detailed description will be given in later sections.
- Hardware module(FPGA)
  Hardware module is the key block of this project; H/W will be designed in Verilog, which is synthesizable and tested robustly. The designed h/w will be ported to Xilinx Spartan-6 FPGA. The h/w will mainly have Memory, DWT processing engine R
- Image post processing block
  The module is will process the output data received from edge detection H/W module which is ported in FPGA. The data will be received from FPGA through hiper terminal application. These data will be rearranged into MxN matrix which will be sent to display unit. This post processing module will be written in matlab.

6. Results

Various functional modules of the design, namely 1D-DWT, 2D-DWT, Pipelined multiplier was presented. A test bench was developed in Verilog so that the design may be functionally verified using Modelsim. First, a Matlab code has been written in order to obtain '.txt' fileform, the data can be read through UART from the computer to input memory. The design is modeled Verilog and synthesized on Xilinx Spartan-6 FPGA

The schematic of area utilization design summary shown in the below represents the how much of area used regarding of area allotted. In this project the Number of Slice Flip Flops available is 18,224used only 745 and 4% of area utilized. Similarly the other parameters related to area as shown in Table 1 and the timing analysis is shown in table 2.

Table 1: Utilization Summary

Logic Utilization	*Used*	*Available*	*Utilization*
Number of Slice Flip Flops	745	18,224	4%
Number of Slice LUTs	1,703	9,112	18%
Number used as AND/OR logic	14		
Number used as logic	1,593	9,112	17%
Number of Block RAM/FIFO	20	32	62%

Table 2: Timing Analysis

Minimum Period	5.72ns
Maximum Frequency	67.92MHz

7. Conclusion

The proposed method is based on new and fast lifting scheme with fully pipelined approach. Pipelining structure in DWT reduces hardware complexity and memory accesses and speeds up the performance. Pipelined Lifting-Based DWT is one such technique which is used to calculate DWT in fewer amounts of time and reduced hardware. The conversion of raw image into Hex format is done using MATLAB and the Hex image is loaded into the FPGA kit. The result of the 2D-DWT provides four filtered images and is passed to display and obtained image retrieve back to the same image using IDWT. The algorithm has been realized in Verilog HDL and implemented using XC6SLX16-CSG324C Xilinx Spartan-6 FPGA device.

8. Future Enhancements

The possible enhancement to the project can be made by extending the single frame to multiple frames. The quality can be further enhanced if higher bit width arithmetic operations are done like Multiplication and addition hardware with 16 bit width versus 8 or 11 Bit width implemented. The design can be extended for bigger resolution image like 256*256, VGA etc. The grayscale image can also be extended RGB images versus current implementation of Gray Scale.

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