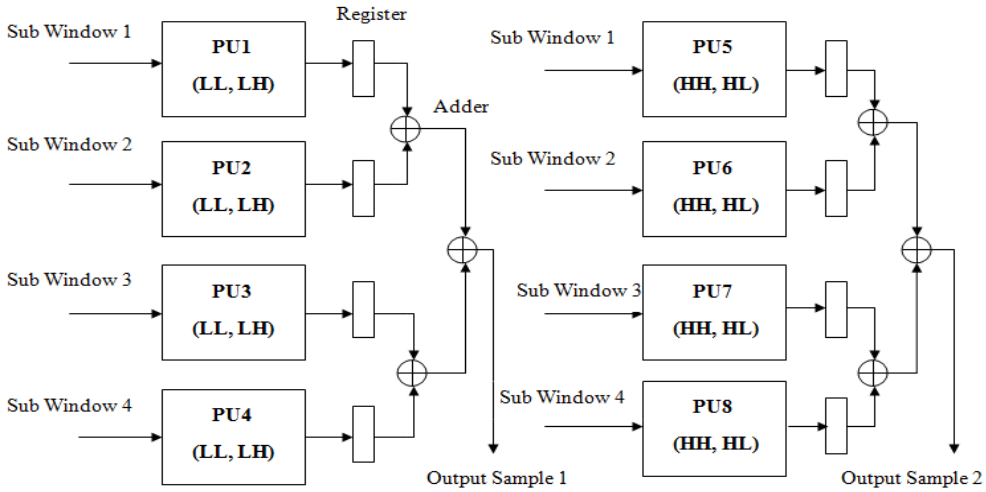

Figure 4: Structure of eight processing units used by stage 1

Stage 2 uses two processing units and the data of the four sub windows 1 to 4 are assigned in a sequential manner to the two processing units. The sub windows 1 and 3 are sequentially given to PU9 and the sub windows 2 and 4 are given to PU10. Figure 5 shows the structure of two processing units used by stage 2. Each of the processing units PU9 and PU10 does the *L/2* x *M/2* tap filtering operations. Here PU9 and PU10 operate in parallel in order to produce the LL, LH, HH and HL sub band samples sequentially in eight consecutive clock cycles.

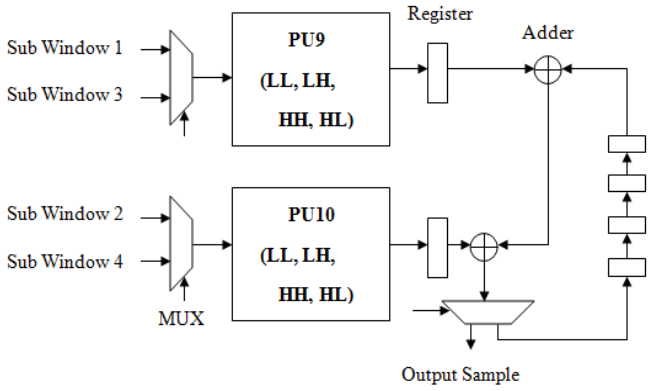

Figure 5: Structure of two processing units used by stage 2

Stage 3 uses only one processing unit, PU11. It carries out all the filtering operations for each of the four sub windows. The four sub windows 1 to 4 are given successively as input to PU11. Figure 6 shows the structure of a processing unit used by stage 3. For each sub window the processing unit PU11 does the *L/2* x *M/2* tap filtering operations. Here PU11 produces the LL, LH, HH and HL sub band samples sequentially in sixteen consecutive clock cycles.

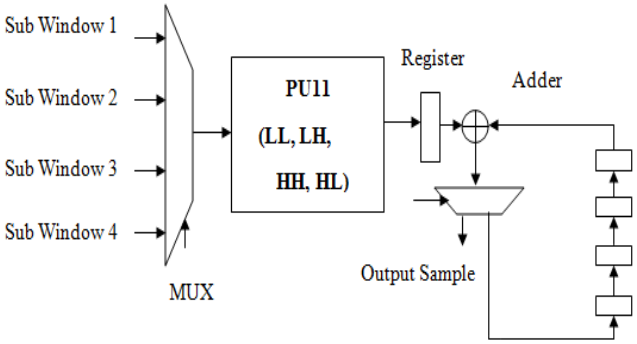

Figure 6: Structure of a processing unit used by stage 3

4.3 Block diagram of the processing unit

We can view the filtering operation carried out by a processing unit as *L/2* x *M/2* parallel multiplications followed by an accumulation of the *L/2* x *M/2* products. Suppose the input samples have a word length of X bits and the filter coefficients have a word length of *Y* bits, then the processing unit will produce an array of (Y * L * *M/4)* x X bits simultaneously in one clock cycle. So to obtain the output sample pertaining to a given sub window the bits of the partial products must be accumulated vertically downward and from right to left by taking into consideration the propagation of the carry bits. Now the partial product bits and/or the carry bits from different rows have to be added. This is done by using bit wise adders in parallel. Then finally we need to add the two rows of bits produced by the accumulation network in order to produce one row of output bits by using a carry propagation adder. Figure 7 shows a block diagram of a processing unit as discussed above.

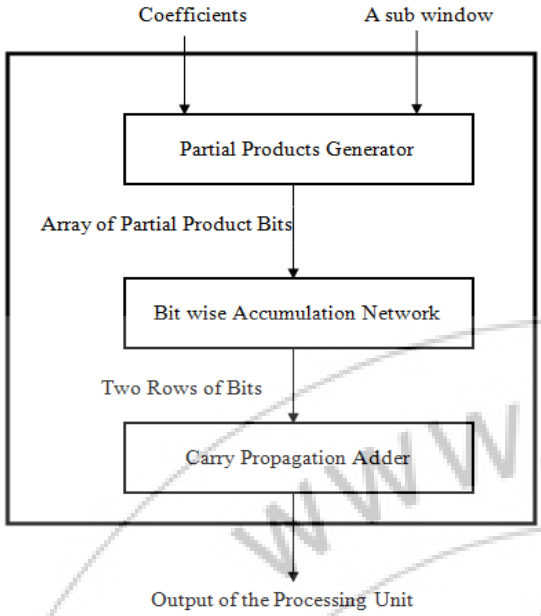

Figure 7: Block diagram of a processing unit

5. Results and Discussion

In order evaluate the performance of the proposed architecture, the code is written for 8x8 input values, simulated, and implemented in FPGA for the 2-D DWT computation. The code is simulated by using Xilinx 14.2 version supported with Isim simulator for three levels of decomposition. The simulation results for one, two and three levels of decomposition are shown in Figure 8, Figure 9 and Figure 10 respectively.

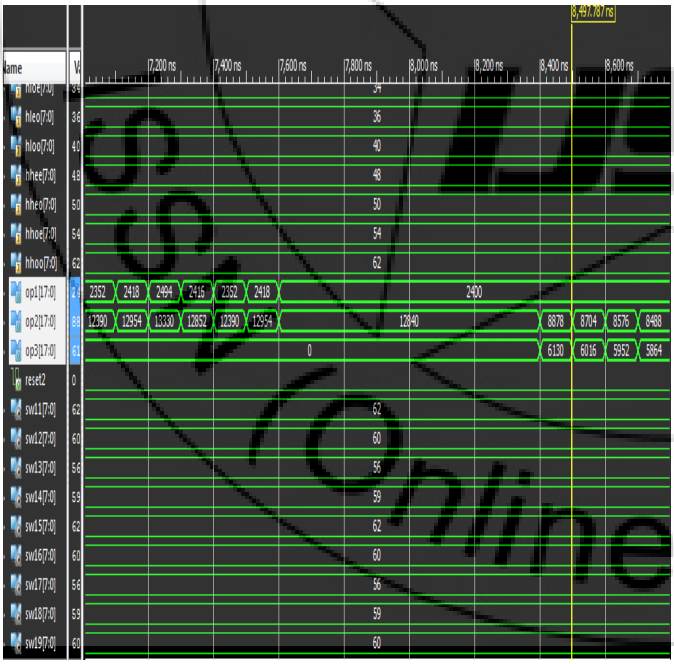

Figure 8: Simulation results for one level of decomposition

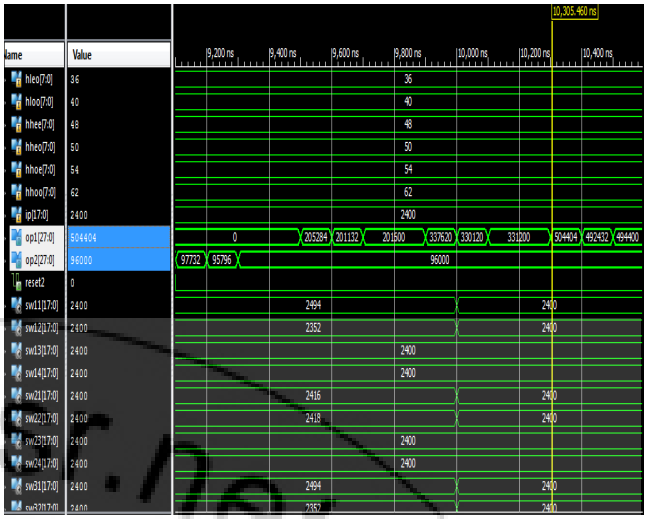

Figure 9: Simulation results for two levels of decomposition

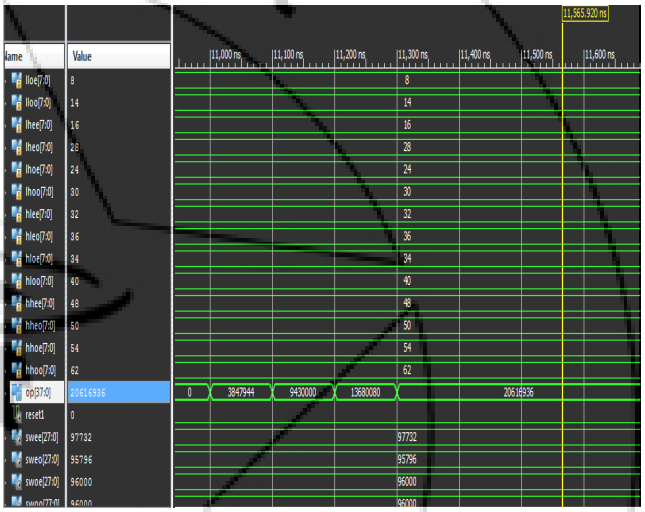

Figure 10: Simulation results for three levels of decomposition

The hardware resources used by the FPGA board Spartan3E XC3S500E-4 in terms of the numbers of configuration logic block (CLB) slices, flip-flop slices, 4-input look-up tables (LUTs) and input/output blocks (IOBs) is shown in Figure 11.

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	3,269	9,312	35%
Number of 4 input LUTs	1,632	9,312	17%
Number of occupied Slices	1,776	4,656	38%
Number of Slices containing only related logic	1,776	1,776	100%
Number of Slices containing unrelated logic	0	1,776	0%
Total Number of 4 input LUTs	1,635	9,312	17%
Number used as logic	1,632		
Number used as a route-thru	3		
Number of bonded IOBs	162	232	69%
Number of BUFGMUXs	1	24	4%
Number of MULT18X18SIOs	14	20	70%
Average Fanout of Non-Clock Nets	2.53		

Figure 11: Device utilization summary for 2-D DWT computation

Also the proposed pipeline architecture is found to perform well with a clock period as short as 17.346 ns (i.e. a maximum clock frequency of 57.651 MHz). When compared to parallel processing architecture the proposed scheme computes the 2-D DWT of a 2-D signal at higher speed.

```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 17.346ns (Maximum Frequency: 57.651MHz)
   Minimum input arrival time before clock: 4.674ns
   Maximum output required time after clock: 4.283ns
   Maximum combinational path delay: No path found
```

Figure 12: Timing Summary for 2-D DWT computation

Table 1: Comparison of proposed scheme with parallel architecture

Type of architecture	*T_c in nanoseconds*
Parallel architecture	17.8
Proposed (Pipeline architecture)	17.34

6. Conclusion

In this paper we have proposed a three-stage pipeline architecture for the real-time computation of the 2-D DWT. The main objective is to achieve a short computation time by maximizing the clock frequency and hence minimizing the number of clock cycles required for the DWT computation. This is done by developing a scheme for enhanced inter-stage and intra-stage computational parallelism for the pipeline architecture. The inter-stage parallelism is improved by optimally mapping the computational task of multi decomposition levels to the stages of the pipeline and then synchronizing their operations. The intra-stage parallelism is improved by dividing the 2-D filtering operation into four subtasks that can be performed independently in parallel. The simulation results for the 2-D DWT computation show that the proposed scheme can operate with a minimum clock period of 17.346 nanoseconds, that is at a maximum frequency of 57.651 MHz. The proposed scheme computes the 2-D DWT at a higher speed when compared to parallel architecture.

References

[1] A.S. Lewis and G. Knowles, "VLSI architecture for 2D Daubechies wavelet transform without multipliers," Electron. Lett., vol. 27, no. 2, pp.171−173, Jan. 1991.
[2] S. Movva, S. Srinivasan, "A novel architecture for lifting-based discrete wavelet transform for JPEG2000 standard suitable for VLSI implementation," in Proc. IEEE 16th Int. Conf. VLSI Design, 4−8 Jan. 2003, pp. 202- 207.
[3] K.C. Hung, Y.S. Hung, and Y.J. Huang, "A nonseparable VLSI architecture for the two-dimensional discrete periodized wavelet transform," IEEE Trans. VLSI Systems, vol. 9, no. 5, pp. 565−576, Oct. 2001.
[4] S. Uzun and A. Amira, "Design and FPGA implementation of non-separable 2- D biorthogonal wavelet transforms for image/video coding," in Proc. IEEE Int. Conf. Image Processing (ICIP), 24−27 Oct. 2004, vol.4, pp. 2825−2828.
[5] C. Chakrabarti and C. Mumford, "Efficient realizations of analysis and synthesis filters based on the 2-D discrete wavelet transform," in Proc. IEEE Int. Conf. Audio, Speech, and Signal Processing, May 1996, pp. 3256–3259.
[6] P. Wu and L. Chen, "An efficient architecture for two-dimensional discrete wavelet transform," IEEE Trans. Circuits and Systems for Video Technology, vol. 11, no. 4, pp. 536 545, Apr. 2001.
[7] J. M. Jou, P. Y. Chen, Y. H. Shiau, and M. S. Liang, "A scalable pipelined architecture for separable 2 D discrete wavelet transform," in Proc. the Asia and South Pacific Design Automation Conf. (ASP-DAC), 18−21 Jan. 1999, vol. 1, pp. 205−208.
[8] K. Mihic, "An efficient semi-systolic architecture for 2-D discrete wavelet transform," in Proc. IEEE European Conf. Circuit Theory and Design (ECCTD), Espoo, Finland, 28−31 Aug. 2001, pp. 333−336.
[9] F. Marino, "Efficient high-speed/low-power pipelined architecture for the direct 2-D discrete wavelet transform," IEEE Trans. Circuits and Systems II: Analog and Digital Signal Processing, vol. 47, no. 12, pp. 1476−1491, Dec. 2000.

Author Profile

Mr. Gopalakrishna K received his B.E degree in Electronics from Dr. Ambedkar Institute of Technology, Bangalore University, Bangalore in the year 1993 and M.Tech degree in VLSI Design and Embedded Systems from VTU. He is awarded with M. Phil degree in Computer Science from M. S. University, Tirunelveli, Tamil Nadu, in the year 2003. He has 21 years of teaching experience in various colleges in India. He is currently working as Associate Professor, Dept. of Electronics & Communication Engineering, School of Engineering & Technology, Jain University. He is pursuing PhD. from Jain University. His field of interests includes Advance microprocessors, Microcontrollers, Embedded Systems, VLSI Technology and VLSI Designing.

Ms. Harshitha S is a student in the Department of Electronics and Communication Engineering, School of Engineering and Technology, Jain University, Karnataka, India. She received her Bachelor degree in Electronics & Communication Engineering from VTU in 2011. She is pursuing M. Tech (SP and VLSI) in Electronics and Communication Engineering, Jain University, Karnataka, India. Her research interest includes Low power VLSI Design, Analog and Mixed mode VLSI Design, CMOS VLSI Design, Embedded Systems Design, DSP and Adaptive signal processing.