In this measurement 4 neighbour's pixel are choosed from the 9 pixels matrix in Medipix2. For each pixel the analog output of the CSA signal is needed. In Figure 4 the four CSA signals from the Medipix2 (A, B, C and D) are fed through coaxial cables to the circuit board.

The summing amplifier is the first part in the circuit architecture it gives the sum of the four input signals. Since the four input resistors and the feedback resistor are equal, the input voltages will be inverted as they are added. As the output signal from the summing amplifier is inverted, second inverting amplifier with unity gain is used. The output pulse is then fed to three comparators (sub sample). The function of the thresholds for the comparators are based on if the signal exceed the threshold value generate clock signal. By setting the global threshold values such that $Th_1>Th_2>Th_3$, the sub-sample is made on this sum by first comparing the magnitude with three global threshold values. As a result sequences of binary events will appear on the outputs of the comparators (U_1, U_2 and U_3). The energy levels of sub-sampled can be made which means that there are two channels (for the ranges Th_1-Th_2 and Th_2-Th_3) for four pixels that are denoted by U_{12} and U_{23}.The decision whether the signal is in U_{12} or U_{23} range is made by two All-Digital Window Discriminator ADWDs modelled in the FPGA.

The second part of the circuit forms the full resolution for the intensity for each pixel. The signals A, B, C and D are the output of the four CSA amplifiers that summed in the summing amplifier; each signal is fed to the two comparators form energy window. The outputs of the comparators (Ua, -Ld) are the clock signals generated depends on the value of the charge signal compared to the threshold, these signals will be fed to the four ADWDs implemented in the FPGA.

The threshold voltages for all comparators in the circuit architecture are controlled by using Labview and DAQ. The VI implemented in Labview has to do two tasks, first to generate continues analogue output by means of voltage to control the threshold for the comparators in the circuit board and secondly to generate clock on digital output channels of DAQ USB-6008 for reset the counters in FPGA.

For continuous analogue voltage two DAQ Express VI`s are used to produce voltages on DAQ USB-6008 analogue output channels, in the case presented by this paper variable voltage is appear on four channels of DAQ USB-6008. The Multifunction DAQ USB-6008 device is connected to the PC via USB port. The voltage can be varied infractions by using Dial Knobs. For generating a fixed clock an array of Boolean values is generated and projected towards digital output channel. The whole VI is enclosed in a single while loop to produce continuous output.

2.3 ADWD and Counter

The ADWD is a digital circuit whose inputs are the sequence of outputs from the comparators. It carries out a window-discrimination function and conditionally generates a clock pulse to the event-counter if the energy is within the window defined by the threshold values given to the comparators. The ADWD is a self-timed circuit that does not rely on any timing assumptions or external timing references. The ADWD is modelled in VHDL based on an asynchronous finite-state machine (AFSM) presented in [7].

The output clock signals of the ADWDs for sub-sample and full spatial resolution are fed to the counters. In order to be able to measure images with a large dynamic range, the capacity of the counters has been implemented in VHDL as 16 bits.

3. Measurement Results

System is setup and an Americium-241 with energy level 59.5 KeV radio isotope is placed in front of the Medipix2 detector, the resultant electrical signal is plugged to the oscilloscope. Figure 5 shows an oscilloscope trace of four CSA pulses.

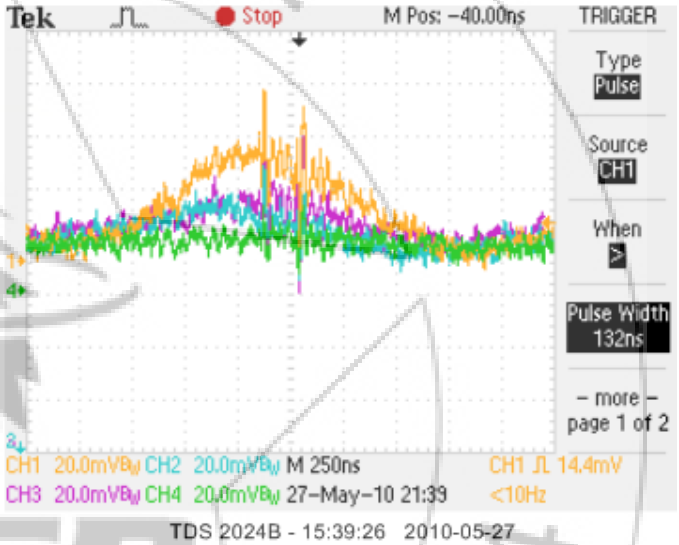

Figure 5: CSA output pulses of a four pixels after exposed Medipix2 to an Americium-241 radioactive source. X=250 ns/div and Y = 20mV/div

Figure 6 shows an oscilloscope photo of the summing amplifier and discriminators outputs. The upper plot represents the summing amplifier output (sum of the 4 outputs of the CSA from Medipix2). The lowers signals are binary signals which are generated by the three comparators with the values of U1 and U2 are high as shown in the Figure and U3 is low. The decision whether the signal is within U12 or U23 range is made by the ADWD is modelled in FPGA

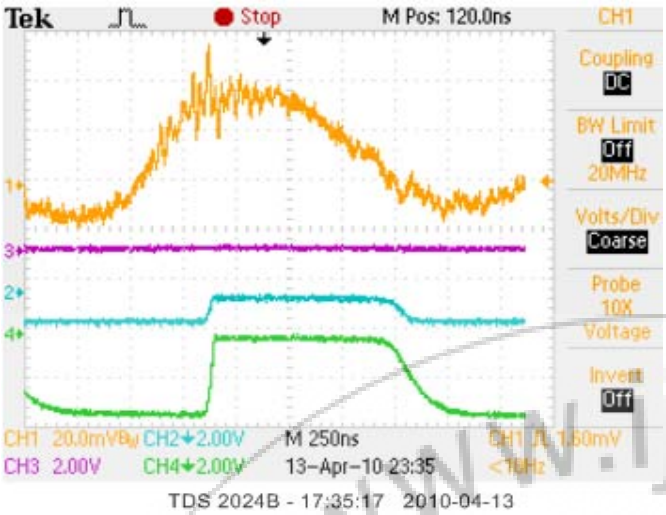

Figure 6: The summing amplifier output with X=250 ns/div and Y = 20mV/div and the lower plots are the comparators digital outputs for sub-sample, with X=250 ns/div and Y = 2V/div

Universal Asynchronous Receiver Transmitter (UART)) module was implemented on the FPGA. The UART module was used to communicate the result of the multiple energy discriminators to a desktop computer for analysis and presentation. An example of the result obtained over UART is shown in Figure 7 and Figure 8. Figure 7 shows counting for an 8-bit system for sub-sample. Figure 8 shows counting for an 8-bit system for full spatial resolution for three counters. This was chosen for ease of analysis on the desktop computer in which the hyper-terminal was set to 8-bit at 9600 baud rate. In the final system, 16-bit colour X-ray counter output will be used and there will be no use for a UART module.

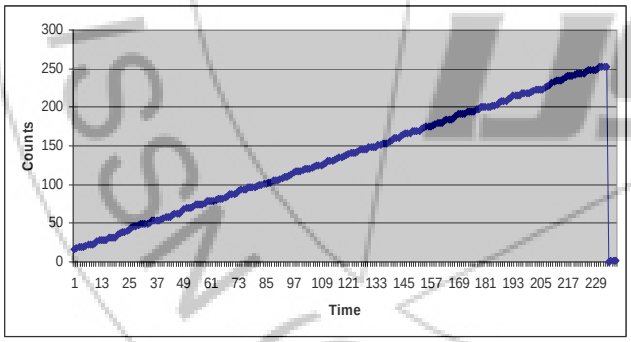

Figure 7: Counter output for sub-sample

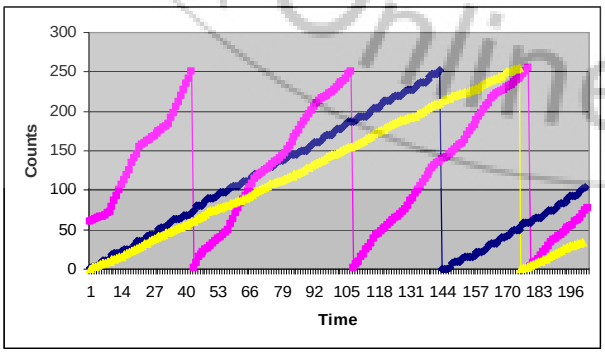

Figure 8: Full special resolution counters outputs for three pixels

4. Conclusion

The presented experiment describes the circuit configuration which is characterized by its optimality and simplicity (high image quality). The technique of sub-sampling was implemented for three-level energy discrimination, that representing the three basic colour component Red, Green, and Blue. Such technique could be used in medical radiology to develop realistic imaging for the deep biological structure.

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Author Profile

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