2.1. Design of 1st order DSM

As the 1st order DSM circuits implementing the BSIM_NMOS and CMOSN mosfets provide the same output responses, the circuit for 1st order DSM using BSIM_NMOS model is considered only.

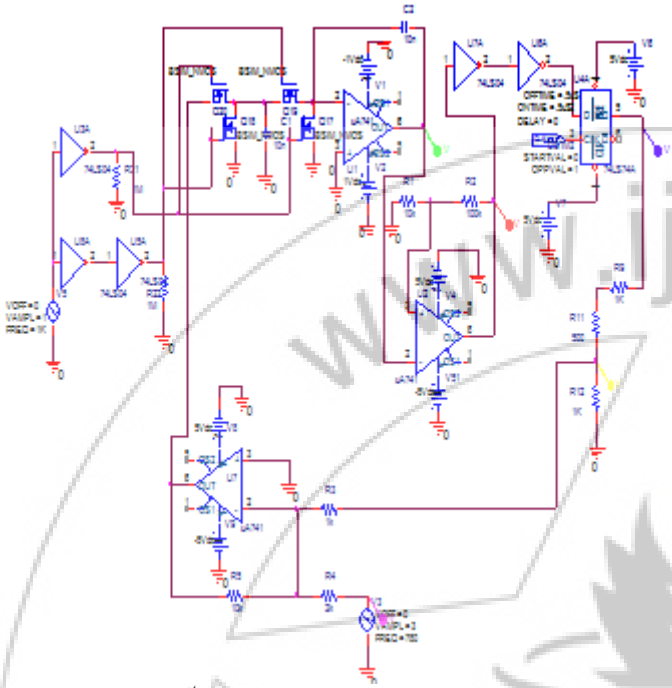

Figure 2.1: 1st order DSM with BSIM_NMOS mosfet

The transient response of figure 2.1 shows the input signal with 3Vpeak-to-peak, the SCI output range is +1V to -.8V, the comparator provides the -1V to +5V, the DAC has an output signal of average 1.2Vto .2V and the FF output is the averaged 3.2V bit stream of 1's with pulse width proportional to the SCI, Comparator and DAC pulses. The input signal and the output bit streams align more as the time forwards.

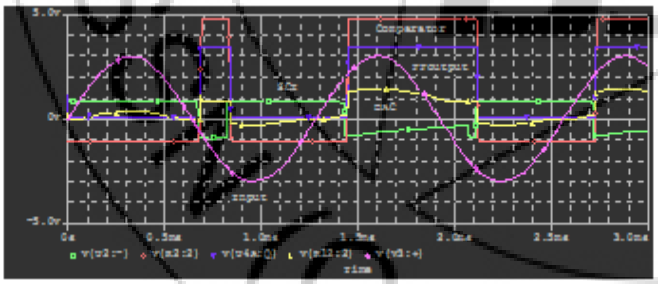

Figure 2.2: Transient response of figure 2.1

The noise signal at the FF output gives the high pass response. The noise is 25mV for the 1st order DSM. Noise is found at 1 KHz. The transient response is same for both the CMOSN and BSIM_NMOS models. So the circuit and responses are only provided for the BSIM_NMOS model.

2.2. Design of 2nd Order Delta Sigma modulator

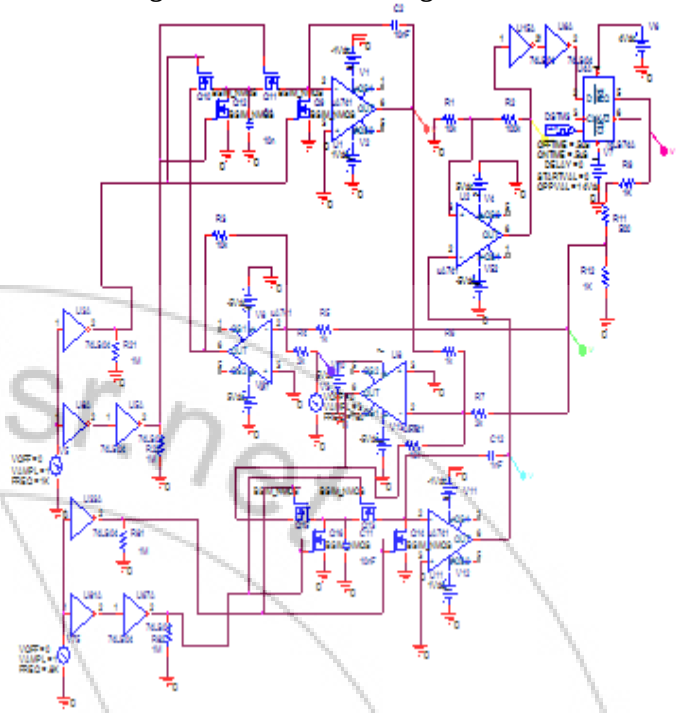

Figure 2.3: 2nd order DSM with BSIM_NMOS

The transient response of the figure 2.3 is shown below. The 1st SCI operates better at 1.4ms and the 2nd SCI at 2ms. The comparator gives 5Vpeak starting at 2ms. The FF outputs bit stream of 1's with 3.2Vpeak. The pulse spread is .2ms.

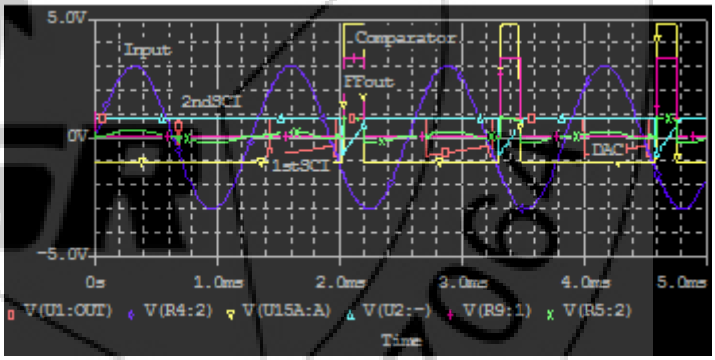

Figure 2.4: Transient response of figure 2.3

The 2nd order DSM schematic design is also done with the CMOSN mosfet. The circuit is as below:

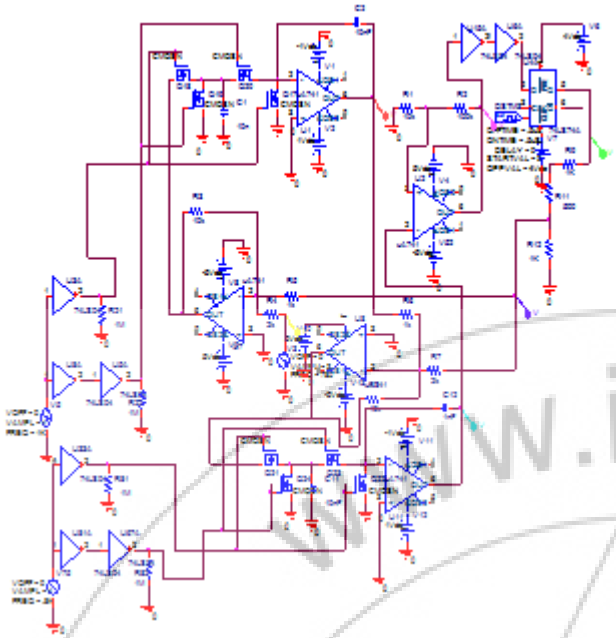

Figure 2.5: 2nd order DSM with CMOSN

The transient response of the circuit shows that the 1st SCI provides better response at 1.42ms and the 2nd SCI at 2ms. The comparator and the FF output is obtained at 2.1ms, the DAC generates error signal at 2ms. That's why the FF starts to output at 2.1ms. The pulse width is .6ms.

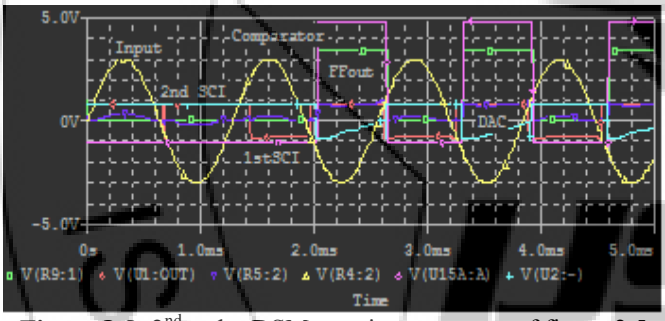

Figure 2.6: 2nd order DSM transient response of figure 2.5

3. Comparison between 1st order and 2nd order DSMs based on Simulation Results

The 1st order DSM consists of a single feedback loop and the 2nd order has two negative loops in its design. Since two different mosfet models are used in the SCI parts for both order, variations are observed which will be discussed below. The clock frequency for both the 1st SCI and the 2nd SCI is 1KHz. The f_o of the 1st SCI is f_o =1/2π*{C1/C2}*fclk; f_o is 1/2π*{10nF/10nF}*1 KHz or 0.16 KHz and for the 2nd SCI, f_o=1/2π*{C1/C2}*fclk= 1/2π*{10nF/1nF}*1 KHz or 1.6 KHz.

3.1 Transient response of 1st order and 2nd order DSMs [output bitstream]

The pulse train starts at .7ms for the 1st order modulator and for 2nd order modulator it starts at 2ms (on avg). This delay is due to the extra feedback loop incorporated in the 2nd order DSM.

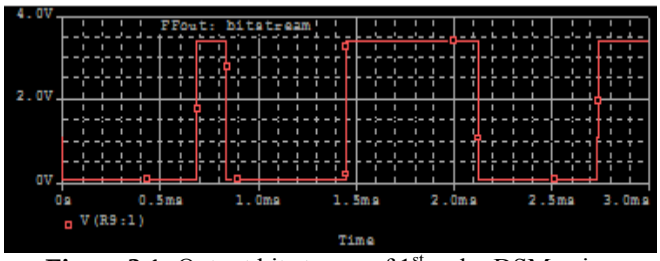

Figure 3.1: Output bit stream of 1st order DSM using BSIM_NMOS model

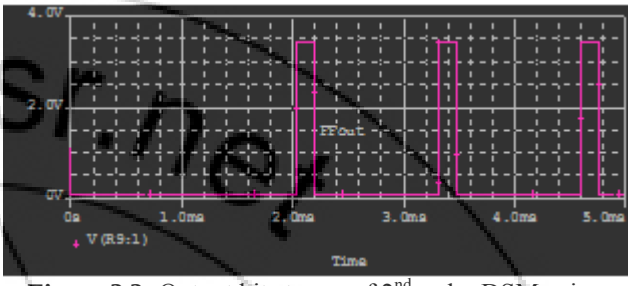

Figure 3.2: Output bit stream of 2nd order DSM using BSIM_NMOS model

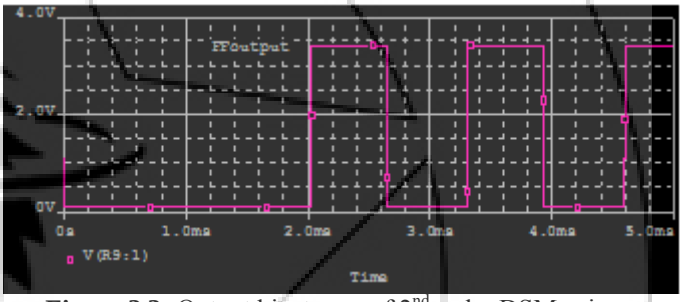

Figure 3.3: Output bit stream of 2nd order DSM using CMOSN model

3.2 Frequency response of 1st order and 2nd order DSMs

The 1st order DSM frequency response is same for the two models. Here the DSM implemented with the CMOSN is considered. The input signal entering the SCI has 30Vpeak amplitude and this low pass frequency dies out at 10MHz. The noise obtained at the FF is **25mV**peak and is generated at 1KHz.

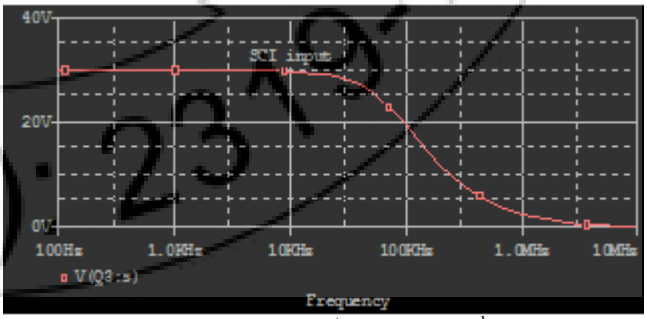

Figure 3.4: SCI Input for 1st order and 2nd order DSM

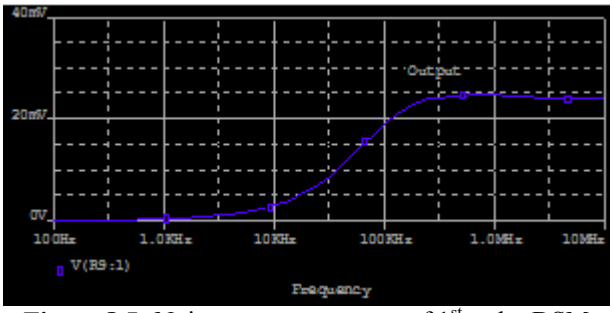

Figure 3.5: Noise present at output of 1st order DSM

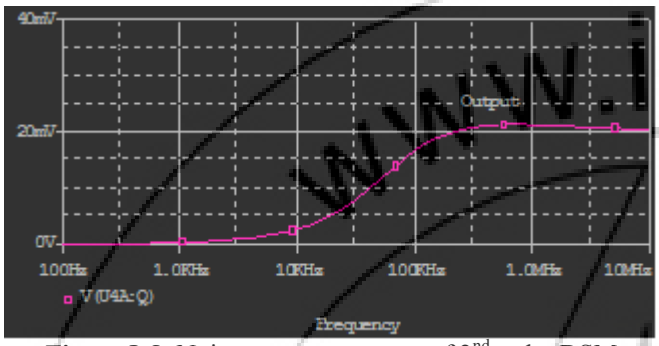

Figure 3.6: Noise present at output of 2nd order DSM

The 2nd order DSM frequency response is also same for the two models. Here the DSM implemented with the CMOSN is considered. The input signal entering the SCI has 30Vpeak amplitude and this low pass frequency dies out before 10MHz. The noise obtained at the FF is **20mV**peak and is generated at 1KHz. So, noise is suppressed better in the 2nd order DSM than the 1st order DSM.

3.3 SCI input of Delta Sigma modulator

The following figure 3.7 is the difference signal present at the input of the 1st order DSM. This difference signal is the result of the analog input signal and the error signal generated by the DAC.

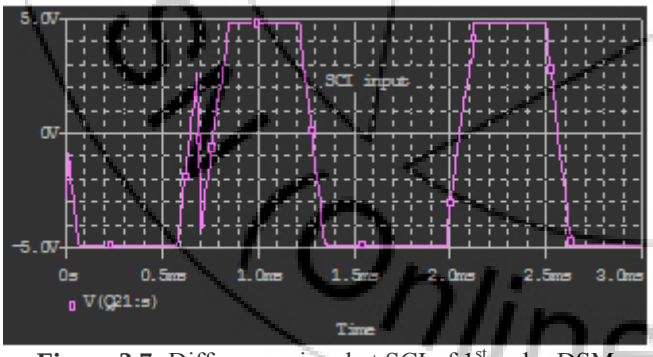

Figure 3.7: Difference signal at SCI of 1st order DSM

The following figure 3.8 is the difference signal present at the input of the 2nd order DSM. The signal is fed at the 1st SCI. This difference signal is the result of the analog input signal and the error signal generated by the DAC.

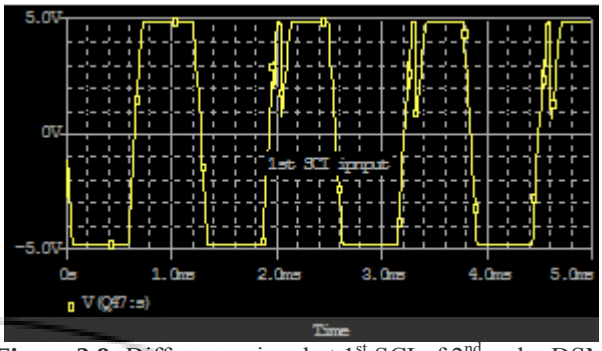

Figure 3.8: Difference signal at 1st SCI of 2nd order DSM

There are spikes in the 2nd order difference signal more than the 1st order DSM. The difference signal appears at the SCI input at .5ms for the 1st order DSM and at .6ms for the 2nd order DSM. This difference in time is due to the extra loop that the signal has to pass through.

4. Conclusion

The Delta Sigma Modulator takes an analog/digital signal as input and produces a pulse proportional modulated signal as its output. The delta sigma modulators designed here are analog ones as they work on a single bit. Two variations based on the order of delta Sigma modulator are designed. The first order single bit delta sigma modulator includes a single feedback loop i.e. one SCI and the second order delta sigma modulator comprise of two-feedback loop and a single comparator. Sampling rate is 2 MHz and the input frequency of 780Hz is taken; over sampling rate is implemented here as the sampling frequency is higher than twice the input frequency. For the same sampling frequency, it has been found that the 2nd order DSM provides more stability and desired output. So, in this paper higher order delta sigma modulator is implemented with the fixed sampling and input frequency to reduce noise rather than employing high OSR. The noise found at the 1st order DSM is 25mV and for 2nd order DSM, it is 20mV. The output of the DSM is the Pulse Proportional Modulated (PPM) signal that is obtained for both the cases of 1st order DSM and 2nd Order DSM while the 2nd order providing reduced noise and better stability. The pulse train generated by the 2nd order DSM using CMOSN model provides proportional bit-stream at output.

The models considered here have not incorporated the white noise parameters. The output bit streams obtained might be different for the BSIMv4 mosfet model if implemented since it has some superior advancement over the BSIMv3.1 model. Implementation of the delta sigma modulator with a low pass analog/digital filter will constitute the widely used delta sigma converter. The modulators can be used in RF band selection, delta sigma converters etc.

References

[1] Traverso, P.A.; Mirri, D.; Pasini, G.; Filicori, F "A nonlinear dynamic S/H-ADC device model based on a modified Volterra series: identification procedure and commercial CAD tool implementation" published in Instrumentation and Measurement, IEEE Transactions on Volume 52, Issue 4, Aug. 2003 Page(s): 1129 – 1135.

[2] Manolis Terrovitis and Ken Kundert, "Device Noise Simulation of ΔΣ Modulators" published by The Designer's Guide Community, Version 1, 24 August 1999.

Author Profile

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