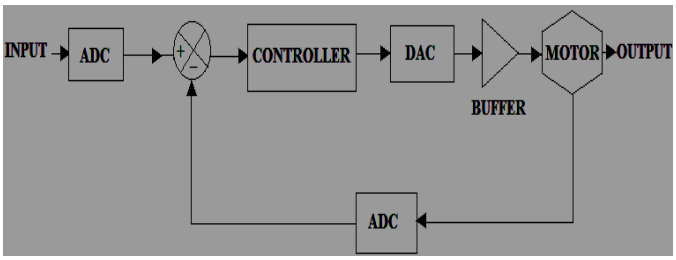

Figure 7: Block diagram of a Digital Control System

The analog input voltage is fed to an analog to digital converter. The output of the ADC sends the corresponding digital signal to the Digital PID controller for further processing. The processed signal is finally fed to the DC motor, which helps to drive the motor.

B. FPGA Implementation

The plant under test is a DC motor which is represented by the following transfer function shown in figure 8.

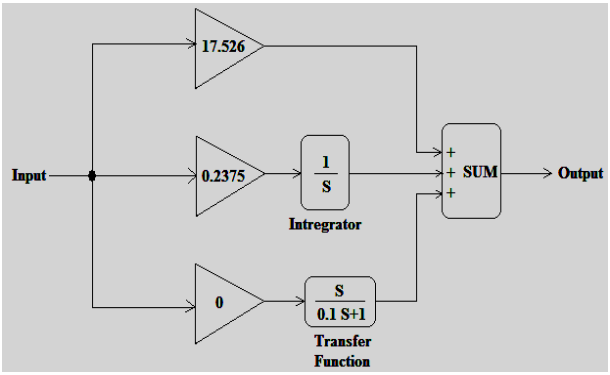

Figure 8: SIMULINK Implementation of PID controller

The speed sensor has a ratio of 0.2; the input signal was 100 mV, representing a desired output speed of 750 revolutions per minute (r.p.m.). The PID parameters for this required output speed are shown in figure 8 by using sampling frequency of 10 KHz [15]. The above PID controller will operate accordingly depending upon the transfer function. The System generator implements the design by considering the correct hardware platform and also takes care of the synchronization and interfacing problems. The flow chart of FPGA implementation is shown in figure 9.

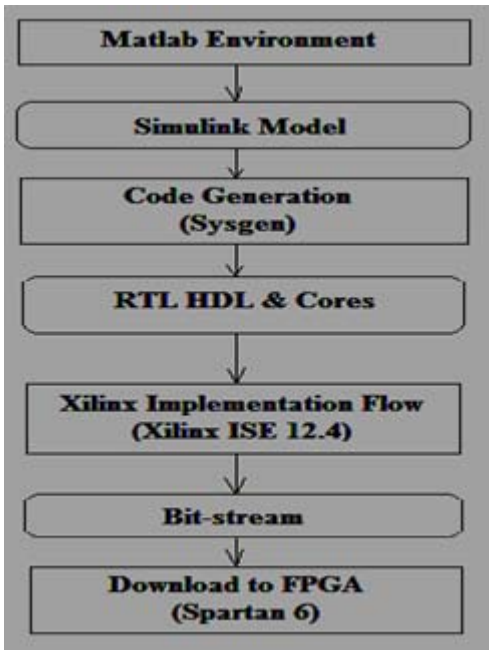

Figure 9: Flow chart of FPGA Implementation

The system generator is Xilinx tool box available with MAT Lab [16]. The blocks used for design and implementation using SysGen are shown below in figure 10.

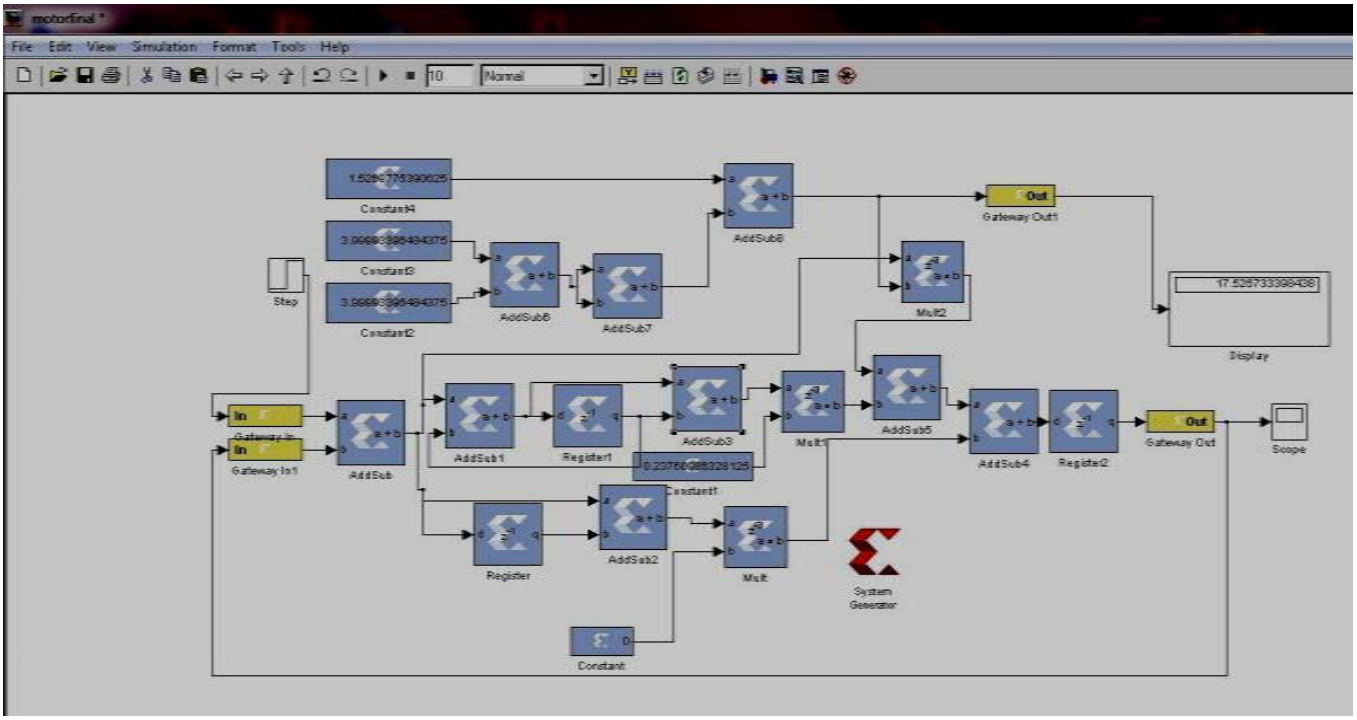

Figure 10: SysGen Implementation of PID controller

Finally the Spartan 6 hardware device processes the input signal from server PC and sends the controlled output signal to drive the DC motor for on/off controlling of the sliding door. Practically this project is fast enough compared to micro-processor based VSS Bio-metric switch (fig. 11).

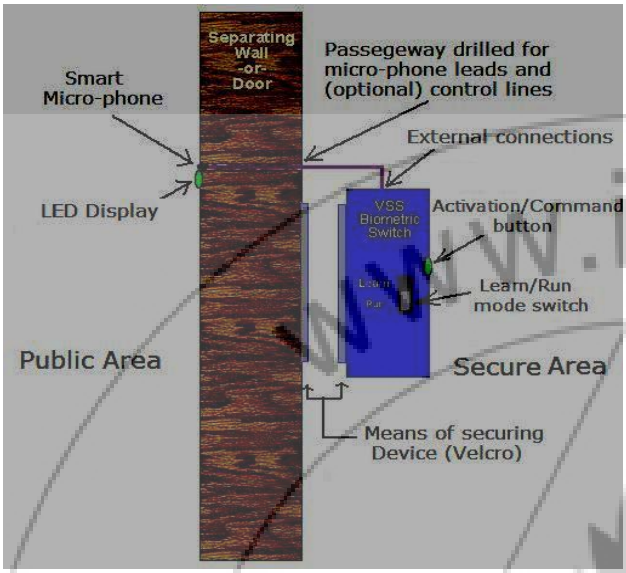

Figure 11: Micro-processor based VSS Bio-metric switch for door control

6. Conclusion

Compared with the micro-processor based door control system, our proposed smart FPGA based system provides fast response as it requires no such delays. Though our proposed system is slightly costly than the earlier one but this new bio-metric system using Spartan FPGA is much faster and more secure than the other secure (speech recognition domain) bio-metric systems. After matching the voice sample with original voice sample a step signal will be sent to the input of the Spartan 6 hardware. Finally the output of Spartan 6 helps to drive the DC motor which mainly controls the open/close of the door of the Security system.

7. Future Recommendations

Now a day's biometric technology such as finger prints [17], voice prints, iris scan [18], face detection [19], signatures or the geometry of the hand are becoming increasingly popular due to the use of unique physical traits. In voice identification technology is still slow to take off in many markets because it is not as accurate as other biometric technologies due to the tendency to have a high flash reject rate because of background noise and other variables. However with the advancement of signal processing technology better vocal synthesis, analysis and measurements using sophisticated algorithms can be taken and converted into a voice print, a unique digital representation of an individual's voice. This technology helps businesses and governments to fight identity threat and fraud, secure transactions, protect confidential information, reduce costs and enhance level of service.

References

[1] Denton J. Daily (2004), *"Programming Logic Fundamentals using Xilinx ISE and CPLDs,"* in Prentice Hall, 203 pages.
[2] Pong P. Chu (2008), *"FPGA Prototyping by Verilog examples: Xilinx Spartan-3 Version"*, Wiley-Interscience.
[3] http://www.xilinx.com/products/silicon-devices/fpga/spartan-6.
[4] Chang J H, Yen J T and Shung K K, *"A novel envelop detector for high frame rate, high frequency ultrasound imaging"*, IEEE Trans. Ultrason Ferroelectr Freq Control, September 2007.
[5] Chi Tsong Chen, *"Digital Signal Processing"*, New York, Oxford University Press, 2003.
[6] Anandthirtha B. GUDI, H. K. Shreedhar and H. C. Nagaraj, *"Estimation of severity of speech disability through speech envelope,"* Signal & Image Processing: An International Journal (SIPIJ), Vol. 2, No. 2, June 2011.
[7] http://www.mathworks.in/help/toolbox/simulink/slref/f4-4889.html#f4-5797.
[8] Alberto Cavallo, Robert Setola and Francesco Vasca, *"Using MATLAB, SIMULINK and Control System Toolbox"*, New York, Prentice Hall, 1996.
[9] http://www.voice-security.com.
[10] E. Shriberg & A. Stolcke (2011), "Language – independent constrained cepstral features for speaker recognition", proc. IEEE ICASSP, pp. 5296-5299, Prague.
[11] Vieira. K, Wilamowski. B and Kubichek. R, "Speaker verification for security systems using artificial neural networks", 23rd International Conference on Industrial Electronics, Control and Instrumentation, 1997 IECON 97, pp. 1102-1107, Vol. 3.
[12] http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,836&Prod=ATLYS
[13] http://www.thinksrs.com/downloads/PDFs/Manuals/SIM960m.pdf
[14] Krikelic, N. J. and Fassois, S. D., "Microprocessor Implementation of PID controllers and lead-lag compensators", IEEE Trans. Industrial Electronics, Vol. IE-31, pp. 79-85, 1984.
[15] I. A. Cosma, V. Maties and C. Rusu, "Control Design and Simulations of the Linear Actuator LX-80-L", SYROM 2009 - Proceedings of the 10th IFToMM International Symposium, DOI.10.1007/978-90-481-3522-6_41, pp. 503-510.
[16] http://www.xilinx.com/training/languages/designing-with-vhdl.htm
[17] F. A. Afsar, M. Arif and M. Hussain, "Fingerprint Identification and verification system using minute matching", Proceedings of National Conference on Emerging Technologies 2004, pp. 141-146.
[18] Weicheng Shen Khanna R., "Prolog to Iris Recognition: An Emerging Biometric Technology", Proceedings of IEEE, Vol. 85, No. 9, September 1997.

[19] Bowyer K. W., "Face Recognition technology: Security versus Privacy", Technology and Society Magazine, IEEE, Vol. 23, No. 1, pp. 09-19, June 2004.

Author Profile

Shivayogi G k received the Bachelor of Engineering from Auden Technology and Management Academy in Electrical and Electronics Engineering from Visvesvaraya Technological University in 2012. His area of interest is Signal Processing, VLSI analog design. Currently perusing Master of Technology in Signal Processing and VLSI from Jain University.

Mavyashree S received the Bachelor of Engineering in Electronics and Communication Engineering from Visvesvaraya Technological University in 2014. Her area of interest is Speech Processing, VLSI analog design, Embedded system