This paper arrange in five sections. Section I Introduction, Section II represents the fundamentals such as Reversible Fredkin gate, and MX-cqca gate. Section III represents testable sequential circuits such as reversible gate based D-latch and reversible gate based Master-slave flip flops and DET flip flop. Section IV shows the simulation results and Section V represents the conclusion.

2. Fundaments of Conservative Logic Based Fredking gate

Conservative logic family consist various gate out of them Fredking gate is universal gate means that by using Fredking gate we solve any types of logical or arithmetical operation [2]. Fig (5) shows the block diagram of 3*3 fredking gate. Which consist of three input terminal (A, B, C) and three output terminal (P, Q, R).

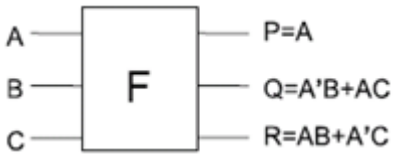


Figure 5: Conservative Logic Based Fredking gate

Fredking gate provide three output out of them last two output is reversible (P=A, Q=A'B+AC, R=AB+A'C) truth table show output of different combination of input.

Truth table of fredking gate

Input			*Output*		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

2.1 Fundaments of MX-cqca Gate

Mx-cqca gate is conservative nature but is not in reversible. This new conservative logic gate is called as Multiplexer conservative logic gate [3]. Because it provide one of the output is same as 2:1 mux.

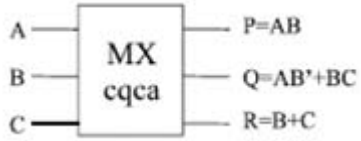


Figure 6: conservative Mx-cqca Gate

Mx-cqca gate consist of three input(A,B,C) and three output (P,Q,R) output p is occurred AND operation of Input A and B Output R is obtained with OR operation between B and C, and output Q obtained with Q=AB'+BC operation.

Truth Table of MX-cqca Gate

Input			*Output*		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	0	1
0	1	1	0	1	1
1	0	0	0	1	0
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	1	1

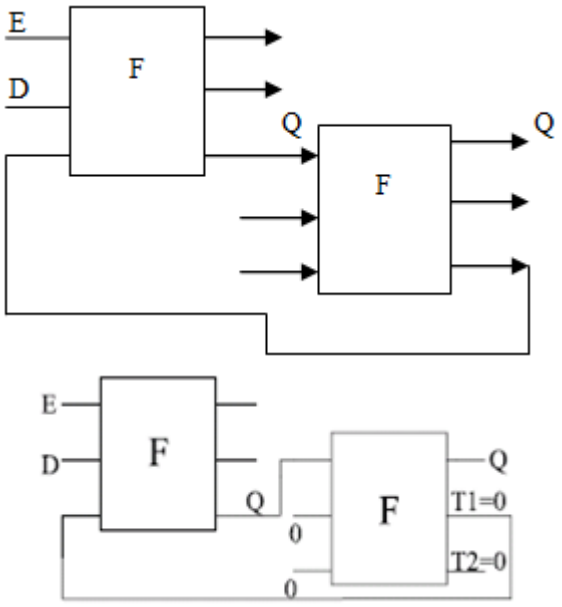
3. Design of Testable Reversible D-latch Sequential Circuit

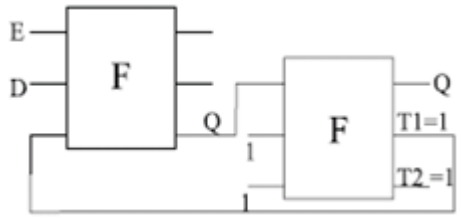
D-latch circuit implemented by using fredking gate. But the design cannot be tested by two input vectors all 0s and all 1s because of feedback and FO problems arrive due to feedback path in test mode. In proposed work clock signal is replace with the Enable signal (E).circuit provide output according to the value of E. When the enable signal (clock) is 1, the value of the input D is reflected at the output that is $Q+ = D$. when $E = 0$ the latch maintains its previous state, that is $Q+ = Q$. Hence characteristics equations is represent as $Q+ = D. E + E. Q$ [4]. The design has operated in two modes with the help of test signal

1)Normal Mode: when C1C2=01 Design circuit perform working operation as a D-latch without introducing any FO problems.

2)Test mode I: When C1C2=00 circuit perform working operation in Test Mode I. It will make the design testable with all 0s input test vectors as output T1 will become 0 resulting testable with all 0s input vectors with Stuck at 1fault.

3)Test mode II: When C1C2=11 circuit perform working operation in Test mode II. It will make the design testable with all 1s input test vector as output T1 will become 1 which find out stuck at 0 fault with all 1s input vector.





(A, B, C) to ($P = A$, $Q = A'B + AC$, $R = AB + A'C$), where A, B, C are the inputs and P, Q, R are the outputs, respectively. The truth table of the Fredkin gate demonstrates that Fredkin gate is reversible and conservative in nature, that is, it has unique input and output mapping and also has the same number of 1s in the outputs as in the inputs.

3.1 Design of Testable Master-Slave Flip-Flops

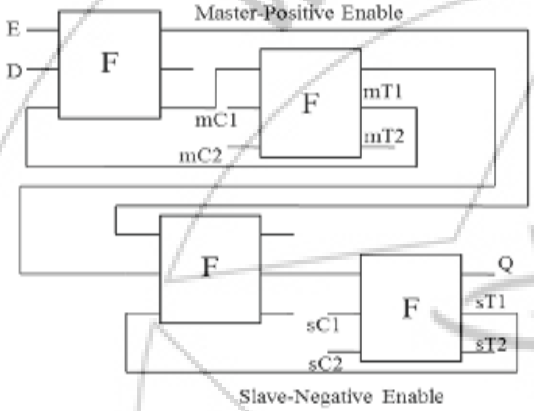


Figure 7

The proposed Master slave flip-flop is design with two clock signals (i.e. positive and negative clock signals) .master part of circuit is design with positive enable D-latch and slave part is design with negative enable D-latch [5].This design is operated in Two Mode with four controlled signal mC1, mC2, sC1, sC2.

Mode of Operation:

1) Normal mode: In the normal mode the control signal status mC1=0, mC2=1, sC1=0, sC2=1.Thus the circuit will do its normal operation. Just operate as a Master-slave operation
2) Test mode (Disrupt the feedback): In the test mode the stuck at 1 and stuck at 0 faults can be found by changing the value of control signal The stuck at 0 fault is found by giving mC1=1, mC2=1, sC1=1, sC2=1, and stuck at 1 fault found by changing value of mC1=0, mC2=0, sC1=0, sC2=0.

3.2 Design of Testable Reversible Det Flip-Flop

In DET flip-flop both clock pulse is used to sample and store input data. This input data is store in falling and rising edge clock pulse [6]. In master-slave flip-flop one disadvantage occur .The disadvantage is that master slave flip-flop does not save input data in both type of clock pulse. This disadvantage recovers with the help of DET flip-flop using reversible concept is proposed for sampling and storing the data at both the edge of the clock cycle. Thus the frequency of DET flip-flop is reduced to half of the master slave flip-flop .Thus for the low power applications these circuits can be used because frequency is proportional to the power.

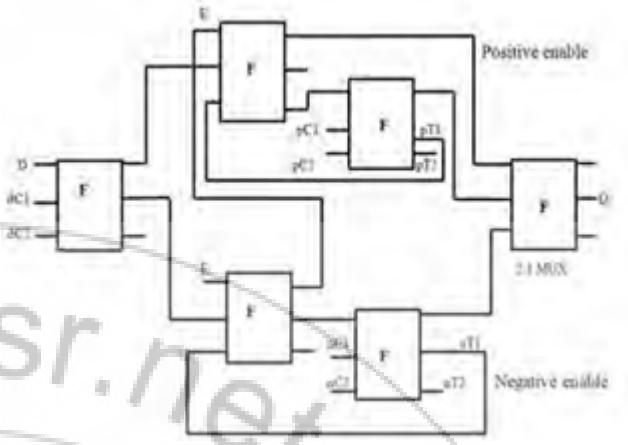


Figure 8: reversible Sequential DET flip-flop

Proposed design of reversible DET flip-flop designed with parallel combination of positive enabled and negative enable D Latch as shown in above fig(8). This circuit also perform the operation in two modes with four controlled signal pC1, pC1, nC1, nC2

1. Normal mode: When value of controlled signal is pC1=0, pC2=1, nC1=0, nC2=1 then circuit operate in normal mode

2. Test mode: In the test mode the stuck at 1 and stuck at 0 faults can be found by changing the control signal value. The stuck at 0 fault is found by giving pC1=1, pC2=1, nC1=1, nC2=1, thus any stuckat-0 fault in the circuit can be identified. Similarly the stuck-at-1 fault is found by giving value opC1=0, nC2=0, pC1=0, nC2=0 thus any struck 1 fault in the circuit can be identified.

4. Stimulation Result

Result 1: D latch Flip-Flop

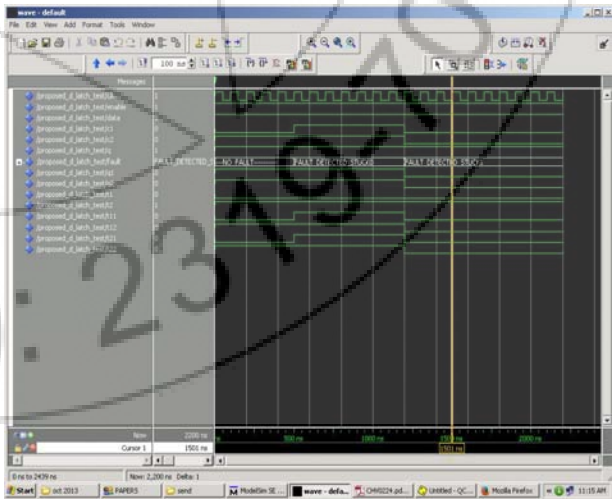


Figure 9: Simulation of testable reversible D latch detecting stuck–at-1 fault and stuck at 0 fault

Result 2: Master-Slave Flip-Flop

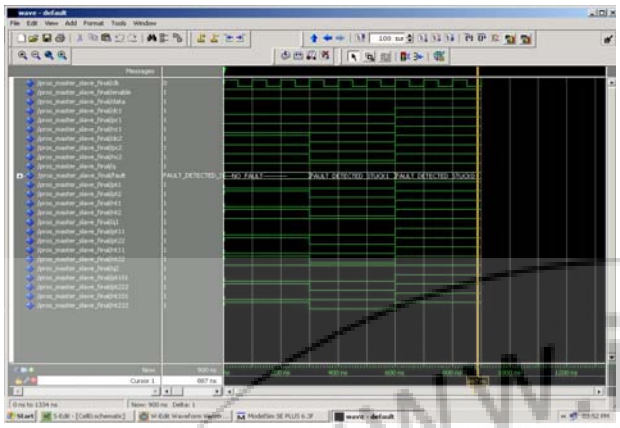


Figure 10: Simulation of testable master slave flipflop detecting stuck-at-0 fault

Result 3: Comparison between Existing and Proposed system

Parameter	*D-Latch*		*Master-slave*	
	Existing	*Proposed*	*Existing*	*Proposed*
Time Delay	3.509ns	3.203 ns	3.704ns	3.229 ns
Power	32 mw	28 mw	29 mw	28 mw
No. of Slice latches	64	2	48	46

C. Related Work

Any nanotechnology having applications of reversible logic, such as based on nano-CMOS devices, low power molecular QCA computing, the research on reversibl1e logic is expanding towards both design and synthesis. Several researchers going with exploring techniques for synthesis of reversible logic circuits and many interesting contributions have been made like area reduction, power dissipation Frequency etc. all are susceptible to high error rates due to transient faults. In this paper we reduced high error rate due to transient fault with the help of MX-cqca Gate on reversible sequential circuits, the design of reversible sequential circuits is addressed in the various interesting contribution in which the designs are optimized in terms of various parameters, such as the garbage outputs, number of reversible gates, quantum cost and delay . To the best of our knowledge, the offline testing of faults in reversible sequential circuits is not addressed in the literature. In this paper, we present the design and test of Digital circuits that can be tested by only two test vectors, all 0s and all 1s, for any unidirectional stuck-at-faults. Further ,the approach of fault testing based on conservative logic is extended toward the design of non reversible sequential circuits based on MX-cqca based on conservative logic is extended toward the design of non reversible sequential circuits based on MX-cqca

5. Conclusion

In This paper proposed work based on Design and Test D-latch, master slave flip-flop, reversible double edge trigger flip-flop by Quantum- Dot Cellular Automata that testing any unidirectional stuck-at faults using only two test vectors, all 0s and all 1s. The proposed all Digital circuits based on multiplexer conservative QCA logic gates (i.e. MX-cqca). In conclusion, this paper advances the state-of-the-art by minimizing the number of test vectors needed to detect stuck-at-faults as well as single missing/additional cell defects. We also reduced power consumption and Area of digital circuit by using Mx-cqca logic gate. We also approached to detect 100% fault tolerance in reversible sequential circuit, while if the same sequential circuit is build using proposed reversible sequential building blocks it can be tested by only two test vectors, all 0s and all 1s. Thus, the main advantage of the proposed conservative reversible sequential circuits compared to the conventional sequential circuit is the need of only two test vectors to test any sequential circuit irrespective of its complexity. The reduction in number of test vectors minimizes the overhead of test time for a reversible sequential circuit. The proposed work has the limitation that it cannot detect multiple stuck-at-faults as well as multiple missing/additional cell defects..

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