shows the clock power dissipation and power reductiondue to supply voltage scaling in two clock networks such as Case1 and Case2 at different frequencies

From table-3 we can see that, if power dissipation inboth clock distribution network is compared there is a noticeable amount of power reduction in clock network with scaled supply voltage(Case2) as compared to clock network with full scale supply voltage(Case1).The main objective of designing such a clock distribution network was power reduction. The power dissipation of clock networks are reduced but a little amount of clock skew introduced due to level converters.

Table 3: Comparison of clock distribution power

Frequency	*Power*	*Power*	*Power*
100MHz	1.12mW	0.53mW	52.15%
200MHz	2.684mW	1.38mW	48.59%
250MHz	3.489mW	1.93mW	44.66%
400MHz	5.895mW	3.62mW	38.6%
500MHz	7.508mW	5.45mW	27.32%
1GHz	14.75mW	10.8mW	26.42%

6. Conclusion

In this brief, we compared the power dissipation in two clock distribution networks,i.e.clock distribution network with full scale supply voltage (Case1)and clock distribution network with scaled supply voltage (Case2) at different frequencies. In Case2 we achieved a significant amount of power reduction than Case1 at each frequency due to scaled supply voltage. Clock signals are reduced from 1.8V to 1.2V during clock distribution and converted back to full scale supply of 1.8V using level converters, such as H.L.L.C(High to Low Level Converter) and L.H.L.C(Low to High Level Converter).We can conclude from these results there is a significant amount of power reduction with supply voltage scaling.

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