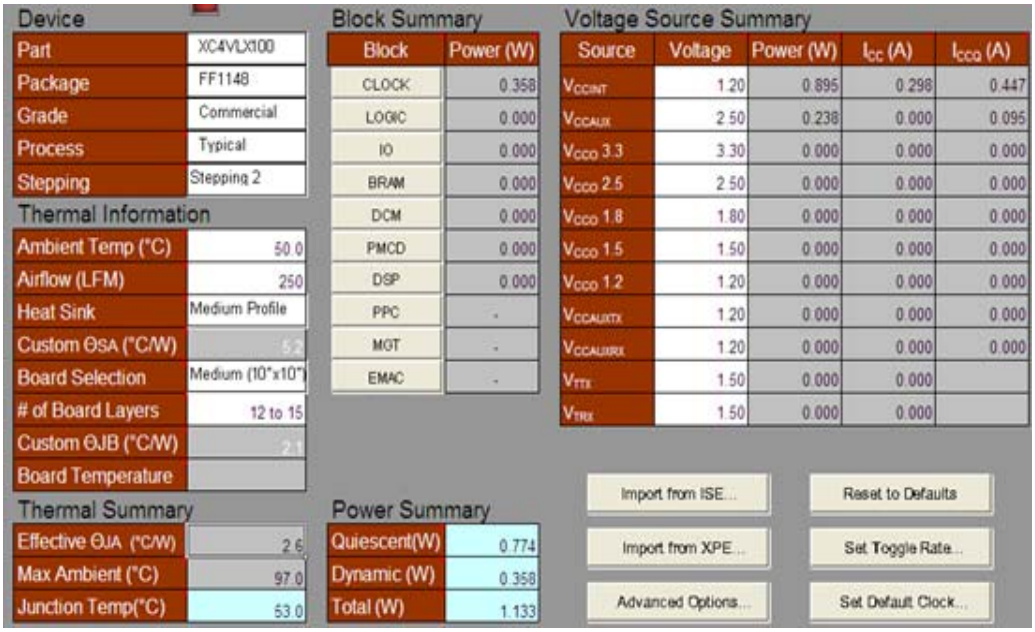

Figure 5: Logic power of radix-2 multiplier

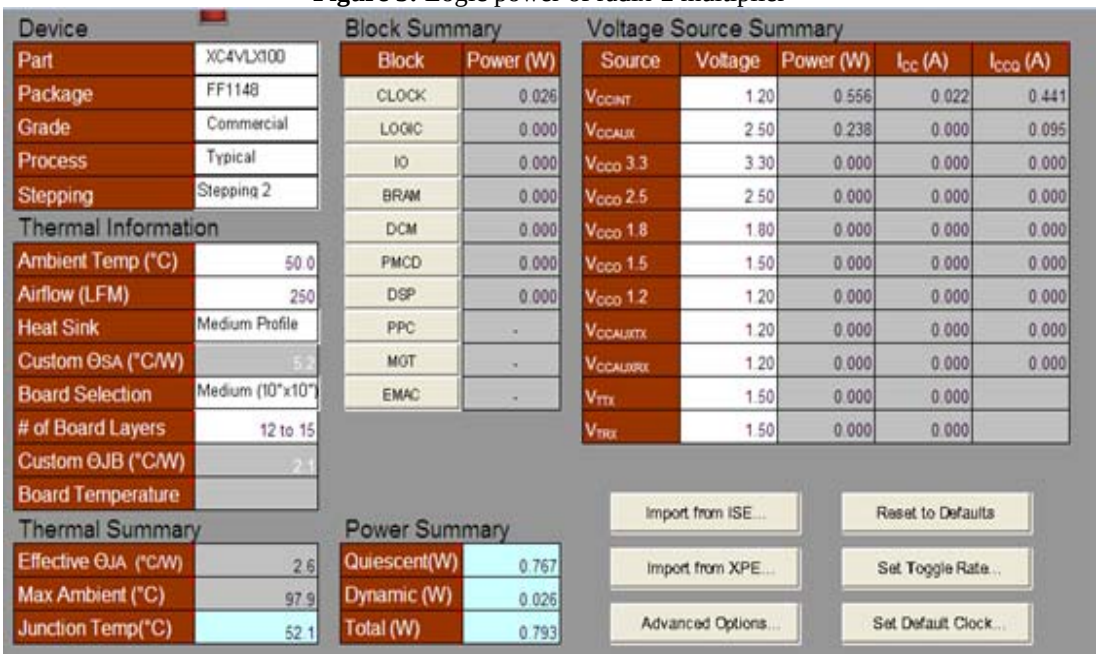

Figure 6: Logic power of radix-4 multiplier

6.2 Output Waveforms

Some output waveforms are obtained by simulating the VHDL coding of different multiplier in Xilinx 9.1.These waveforms are shown in following figures 7, 8, 9.

Figure 7: Output waveform of shift and add multiplier

Figure 8: Output waveform of radix-2 multiplier

Figure 9: Output waveform of radix-4 multiplier

7. Conclusion and Future Work

7.1 Conclusion

This paper work gives a clear description of different multipliers and their implementation in tap delay finite impulse response (FIR) filter. After simulation, we found that the parallel multiplier (radix-4) are much faster than the serial multiplier (shift and add multiplier). We also found the power consumption of different multiplier using power estimator tool. According to our result parallel multiplier (radix-4) has the low power consumption as compare to serial multiplier (shift and add multiplier).

In comparison of radix- 2 and radix-4 Booth multiplier, we found that the radix- 4 multiplier consumes less power than the radix- 2 multiplier, because it uses almost half the number of iterations and the adder compared to the radix-2. When all three multipliers were compared, we found that array multiplier is the most power consuming, and has the largest area. This is because it uses a lot of adders. Therefore, it will slow down the system because the current system has done a lot of calculations.

Various digital multipliers are one of the most important system components for designing different types of digital systems. Therefore, a better solution for the multiplier is to be found out. We should always ensure that multiplier consumes less power and has small coverage area. So through our dissertation work, we tried to determine which of the three algorithms works best. Finally, we show that the radix-4 multiplier is better in terms of power and speed for the design of digital circuits.

7.2 Future Work

As an attempt to develop arithmetic algorithm and architecture level low power optimization techniques for multiplier design, research presented in this paper has achieved good results, showing a high level of efficiency and optimization techniques. However, there are limitations but some of our work and future research directions are possible. One probable direction is higher than the radix -4. We only took into consideration the radix _ 4 multiplier, because it is a simple and popular choice. To further decrease the number of multiplication and adders higher radix is used, and thus has low power consumption. Another possible direction may be parameters such as a symbol - in the form of amplitude or compliment, which in whichever case prove to be low power consuming, less time consuming and has high speed.

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