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Low Power 8 Bit quantum ALU Implementation Using Reversible Logic Structure

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Abstract: ***Reversible computation emerged as a result of the utilization of quantum mechanics principles in the development of a universal computing machine. Reversible computing has a strong impact on digital logic designs. Reversible logic units are required to recover the state of inputs from its outputs. It will have an impact on instruction sets and high-level programming languages as well. Finally, these will also have to be reversible to produce optimal efficiency. Upcoming advancements in reversible logic allow new methods for computer architectures using improved quantum computer algorithms. Important contributions have been made in the literature based on the design of reversible logic gate structures and arithmetic units, however, there are not many efforts directed towards the design of reversible ALUs. In this work, novel programmable reversible logic gates are presented and utilized, and its implementation in the design of a reversible Arithmetic Logic Unit is illustrated. Using 1 bit ALU, an 8 bit ALU has been designed and verified. This proposed 8 bit ALU is also compared against the existing 8 bit ALU with reference to few important parameters such as power dissipation and propagation delay. The major advantage of proposed ALU is the increased number of operations with certain number of select inputs with low power consumption. This ALU can be utilized in low power VLSI design, nanotechnology, quantum computing and optical computing.***

Keywords: Quantum computing, Reversible logic structures, Arithmetic logic unit, VLSI, Low power dissipation.

1. Introduction

Reversible logic has intense potential to have extended applications in future emerging technologies. Reversible logic is very useful for the construction of low power, low loss computational structures which are very much significant for the construction of arithmetic circuits used in quantum computation, nanotechnology and other low power digital circuits. Nowadays, several researchers have directed their efforts on the design and synthesis of efficient reversible logic circuits. The most important reversible gates used for reversible logic synthesis are Feynman Gate, Fredkin gate, HNG gate and MG gate.

2. Reversible Logic

Reversibility means that no relative information about the computational states can ever be lost, so we can recover at any earlier stage by computing in backward direction or un-computing the results. This is said to be logical reversibility. A reversible logic gate is a k-input and k-output (k*k) device that maps each possible input vector pattern into a unique output vector pattern as shown in fig.1 where I0,I1,I2,….IK-1 are the input vectors and O0,O1,O2,…..OK-1 are the output vectors.

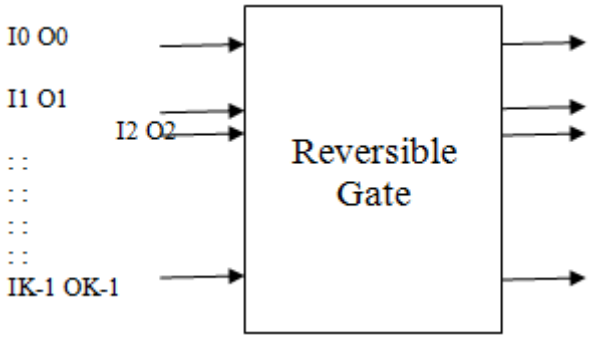

Figure 1: General structure of reversible gate

3. Reversible Gates

A reversible logic gate is an n-input and n-output logic device having one-to-one mapping. This helps to determine the outputs from their inputs and also the inputs can be uniquely and successfully recovered from the outputs.

The Feynman gate is the basic fundamental reversible logic gate. It functions as a two input reversible gate with outputs P = A and Q = A XOR B. The gate flips the target qubit if and only if the control qubit is 1. The resulting value of the second qubit corresponds to the result of a conventional XOR gate. When the second input is 0, the Feynman gate may be used to produce a duplicate of input signal. Its quantum configuration is shown in figure 2.

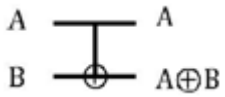

Figure 2: Quantum representation of Feynman gate

The integrated 2*2 qubit gate is obtained by implementing a Feynman gate with either a Controlled-V or Controlled V+ gate. The XOR output of the Feynman gate functions as the control input of the Controlled-V or V+ gate. Its quantum cost is taken as 1, and is shown in figure 3.

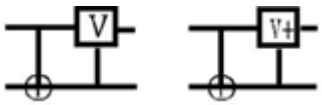

Figure 3: Quantum representation of integrated Qubit gates

The Fredkin gate is a 3*3 reversible logic gate whose quantum representation is shown in figure 4. The outputs are related with the inputs as follows: P = A, Q = A'B+AC and R = AB+A'C. Therefore, the outputs works as a multiplexed

output of the two data inputs based on the control input. It is constructed using 2 Feynman gates, a Controlled-V gate and two integrated qubit gates.

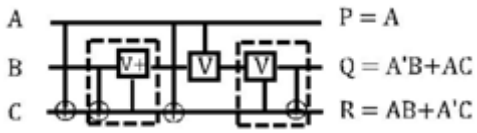

Figure 4: Quantum representation of Fredkin gate

The Toffoli gate is a 3*3 reversible logic gate whose quantum representation is shown in figure 5. The outputs map to the inputs in this manner: P = A, Q = B and R = AB XOR C.

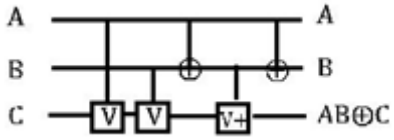

Figure 5: Quantum representation of Toffoli gate

The Peres gate is a 3*3 reversible logic gate whose quantum representation is shown in figure 6. The outputs are related with the inputs in this manner: P = A, Q = A XOR B and R = AB XOR C.

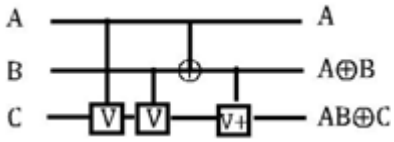

Figure 6: Quantum representation of Peres gate

4. One Bit ALU Implementation

We propose the design of a 5*5 programmable reversible logic gate structure utilized in the implementation of an ALU. The cost of the MG is 7, and the worst-case delay is 7. The truth table of MG gate is given below which shows the operations obtained according to combinations of select inputs.

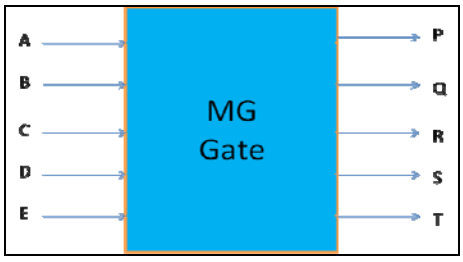

Figure 7: Block diagram of MG gate

MG gate has 5 inputs i.e. A, B, C, D, and E and 5 outputs i.e. P, Q, R, S, and T. Output vectors have following expressions: P = A, Q = A XOR B, R = (A XOR B) XOR C, S = AB XOR D and T = ((A XOR B) XOR E) XOR (AB XOR D)

Table 1: Truth table of MG gate

C	D	E	R	S	T
0	0	0	A XOR B	A AND B	A OR B
0	0	1	A XOR B	A AND B	A NOR B
0	1	0	A XOR B	A NAND B	A NOR B
0	1	1	A XOR B	A NAND B	A OR B
1	0	0	A XNOR B	A AND B	A OR B
1	0	1	A XNOR B	A AND B	A NOR B
1	1	0	A XNOR B	A NAND B	A NOR B
1	1	1	A XNOR B	A NAND B	A OR B

The MG gate is utilized in the implementation of a novel arithmetic logic unit. The ALU, in addition to producing the same logical calculations as the MG, is able to perform addition and subtraction by utilizing the HNG gate and store less-than operation.

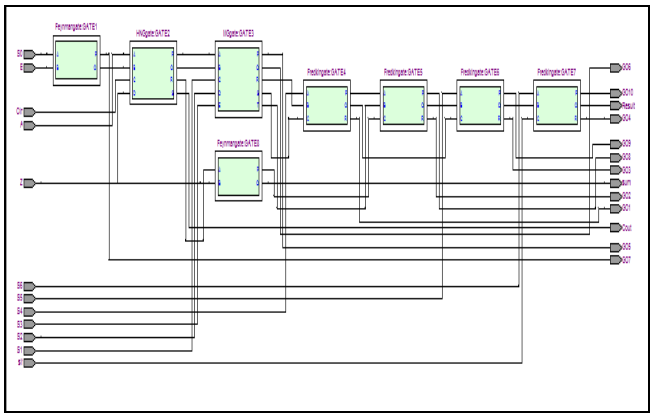

Figure 8: RTL view of 1-bit ALU

The operation code of 1-bit ALU is shown below which represents eight operations with certain combinations of six select inputs.

Table 2: Operation codes of 1-bit ALU

Select Inputs							Hex Code	Operation
S6	S5	S4	S3	S2	S1	S0		
0	1	1	0	0	0	0	30H	AND
0	1	1	0	1	1	0	36H	NAND
0	0	0	1	1	0	0	0CH	OR
0	0	0	0	1	1	0	06H	NOR
0	1	0	0	1	0	0	24H	XOR
0	1	0	0	1	1	0	26H	XNOR
0	0	1	1	0	0	0	18H	ADD
0	0	1	1	1	0	0	1CH	SUB

5. Eight Bit ALU Implementation

By using 1-bit ALU described above an 8-bit ALU has been designed and verified. This 8-bit ALU will also produce the same operations on two 8-bit inputs as in case of 1-bit ALU. The 8-bit ALU reflects the select input combinations for 8-bit vector inputs generating same results.

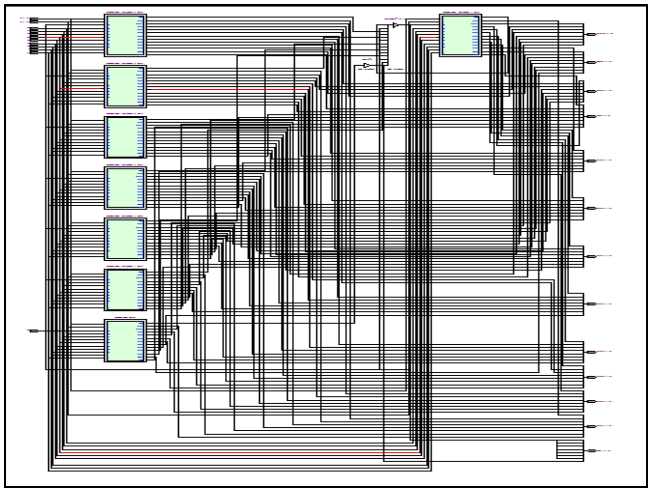

Figure 9: RTL view of 8-bit ALU

6. Simulation Results

The 1-bit ALU and 8-bit ALU are simulated and their simulated waveforms are verified by using QUARTUS II simulation software in VHDL. The simulation results of 1-bit ALU is shown below where select inputs S4 and S5 taken as logic 1 while other select inputs taken as logic 0. This makes the op-code as 30H which indicates AND operation as mentioned in operation codes of 1-bit ALU. The complete AND operation truth table has been verified by its functional simulation as shown in figure.

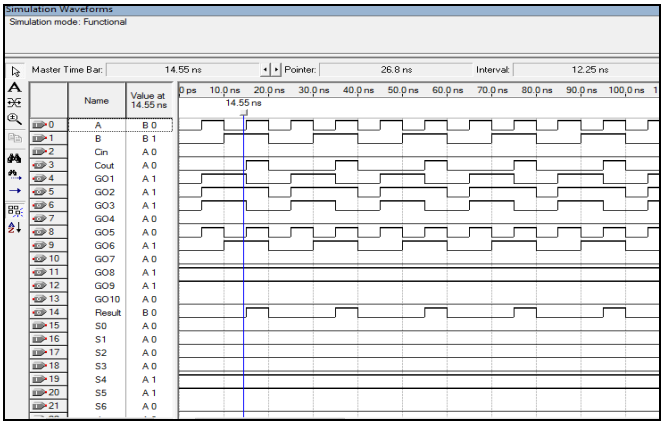

Figure 10: Simulation waveforms of 1-bit ALU

The simulation result of 8-bit ALU is shown in figure below where select inputs S3 and S4 taken as logic 1 while other select inputs taken as logic 0. This makes op-code as 18H which indicates ADD operation as mentioned in operation codes of 8-bit ALU. The complete ADD operation can be verified by its functional simulation as shown in figure below.

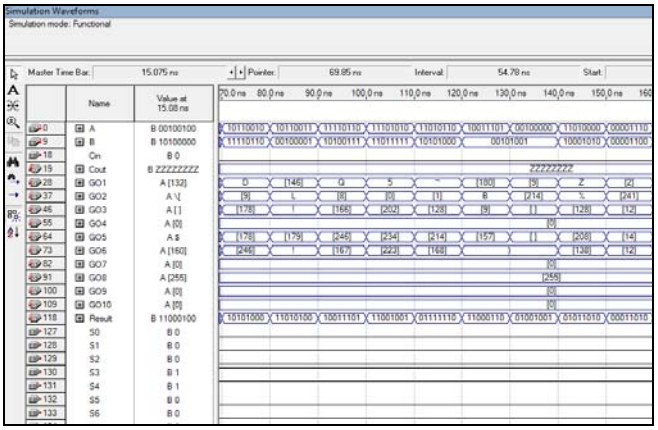

Figure 11: Simulation waveforms of 8-bit ALU

7. Comparison

The comparative analysis of proposed ALU with respect to the existing ALU is given below. This comparison is mainly based upon important parameters such as power dissipation and propagation delay.

Table 3: Comparative analysis of 8-bit ALU

Sr. No.	Parameters	Existing 8 bit ALU1	Proposed 8 bit ALU
1	Total thermal power estimate	270.78 mW	265.81 mW
2	Core dynamic power dissipation	18.49 mW	14.71 mW
3	Core static power dissipation	39.63 mW	39.63 mW
4	I/O thermal power dissipation	212.66 mW	211.48 mW
5	Max. propagation delay	9.270 ns	19.506 ns
6	Min. propagation delay	3.015 ns	4.092 ns
7	Number of operations	6	8

After analyzing the above comparison we can conclude that the proposed ALU is more power efficient than the existing one at the cost of slight increase in propagation delay.

8. Conclusions

A novel 5*5 programmable MG gate was proposed and verified that may calculate of AND, NAND, OR, NOR, OR and XNOR depending on the inputs from the programmer. The proposed MG gate has been implemented in the design of a novel quantum arithmetic logic unit, and its design has been compared with the existing work in programmable ALU design. The novel 1-bit ALU required only minimal increase in quantum cost and delay due to the MG design, which also allowed for increased functionality for the computing machine. An ALU is a major component of a computing device and is the core component of central processing unit. Moreover, it is the heart of the instruction execution portion of every computer. An ALU is a multi-functional circuit that conditionally performs one of several possible functions on two operands A and B depending on the combinations of selection inputs. The low power dissipation of proposed ALU makes it more useful in less power requirement applications.

9. Future Scope

This ALU can be used in applications such as quantum computing, nano-technology, optical computing, low power VLSI designs etc. The extended operations will be more useful for doing complex logic designs. Many ASICs based projects could be possible by using the proposed ALU design.

10. Acknowledgement

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