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Design and Implementation of Efficient Multichannel Data Compression in Wireless Sensor Nodes

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Abstract: ***Recent technological advances in sensors, low-power integrated circuits, and wireless communications have enabled the design of low-cost, miniature, lightweight, and intelligent physiological sensor nodes. These nodes, capable of sensing, processing, and communicating one or more vital signs. Implementing a system designed with PIC microcontroller to collect the raw analog data from the multi channel. It digitalizes the data and compresses the data according to the desired sample rate and bit resolution. The realization of a multichannel data compression system by using all digital method has the characteristics of high reliability, strong anti-disturbance, good flexibility and convenient for application. Results of the analysis show that a digital implementation is significantly more energy-efficient for the wireless sensor space where signals require high gain and medium to high resolutions.***

Keywords: PIC, Analog to Digital Converter, Data compression, wireless sensor node

1. Introduction

Wireless nodes are responsible for sensing, processing and monitoring environmental data. The wireless nodes collect environmental data such as temperature, pressure, position, flow, humidity, vibration, force and motion to monitor the real-world. There are limiting parameters on WSNs such as power consumption, lifetime, delay, size, bandwidth, signal distortion and cost and global traffic. With the development of the high-speed large scale integrated circuit, data compression can be implemented in digital method. It can decrease the size of the system and it also has high stability and maintainability, and this can improve the programmable ability of the system. So the digital processing method is of catholic concern and has been widely applied. Existing strategies for implementing integrated data compression or filtering solutions under these constraints largely revolve around detecting and extracting specific signal data However, the filtered data often contains limited information. For example, in neural recorders, the data is typically limited to just the time and amplitude of a neural spike event rather than the signal itself. Even when the event detection is used to trigger a full signal capture, the system is susceptible to missing events entirely if detection thresholds are not properly set. Meanwhile, feature extraction approaches require training, are usually signal specific and typically provide only macro level decisions based on the original signals. For these signal processing strategies, there is a tradeoff between data reduction, robustness, implementation cost, and the granularity of information captured. In each case, the goal is to minimize the number of bits transmitted (to minimize the average radio power) while reliably preserving the signal information at a minimum implementation cost.

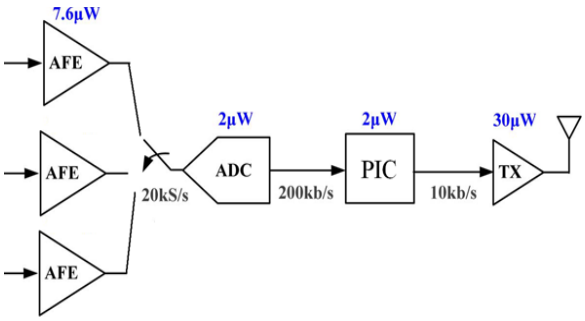


Figure 1: System design

In this work, we introduce the design and implementation of a PIC16F84A architecture based on the theory of compressed sensing that offers an improved set of tradeoffs toward achieving this goal. This system combines the positive qualities of existing data acquisition and compression systems: it provides a flexible and general interface like an analog-to-digital converter (ADC), yet still enables data compression proportional to the signal information content, which is consistent with the performance of source coding. Traditional data acquisition architectures have been based on the principles of Shannon's sampling theorem which requires that the sampling rate must be greater than twice the maximum frequency of the signal being sampled. Compressed sensing is an emerging field whose theory leverages known signal structure to acquire sampled data at a rate proportional to the information content rather than the frequency content of a signal. In theory, this would enable far fewer data samples than traditionally required when capturing signals with relatively high bandwidth, but a low information rate. As shown in Table I, many biophysical signals of interest fall into this category where their required sampling rates far exceed the information rate (frequency of event occurrences). Although these examples are in the context of medical applications, they can be generally applied to any field where the signals of interest are sparse. For data compression we need to convert the analog signal to digital converter (ADC). Digital data compression processing of the linear FM usually adopts the double channels of

perpendicular processing scheme to avoid the effect of Echo Signal's random-phase, which may reduce the loss of system processing by about 3dB; meantime, this method can reduce the demand for AD acquisition devices. The current PIC has been becoming the core component of digital system. In the chip, it includes not only the logical resources as well as multiplexers, memory, hard-core multiply-add units and other equipments, but also can be provided with the ability of highly parallel computing. which has made PIC become the ideal device of high performance digital signal processing, particularly suitable for completing digital filtering, fast Fourier transform etc.

The structure of the paper is as follows.

Section II Wireless Sensor node background.
Section III The chosen Software
Section IV The system function and structure.
Section V Discussion and Section VI gives the simulation and implementation results.

Table 1: Characteristics of Common Measured Bio-Signals

Signal	Sampling Rate	Frequency of Events	Event Duration	Duty Cycle (%)
Extracellular APs	30 kHz	10– 150 /s	1– 2 ms	2 to 30
EMG	15 kHz	0– 10 /s	0.1– 10 s	0 to 100
EKG	250 Hz	0– 4 /s	0.4– 0.7 s	0 to 100
EEG, LFP	200 Hz	0– 1 /s	0.5– 1 s	0 to 100
O_2, Ph, Temp	0.1 Hz	0.1 /s	N/A	Very low

2. Wireless Sensor Node Background

Wireless Sensor Node has opened the doors to many applications that need monitoring, processing and control. A WSN system is ideal for an application like environmental monitoring in which the requirements mandate a long-term deployed solution to acquire water, soil, or climate measurement. For utilities such as the electricity grid, streetlights, and water municipals, wireless sensors offer a lower-cost method for collecting system data to reduce energy usage and better manage resources. WSN is used to effectively monitor highways, bridges, and tunnels. This section presents the basic theory of WSN and its limiting characteristics such as power and delay in wireless nodes.

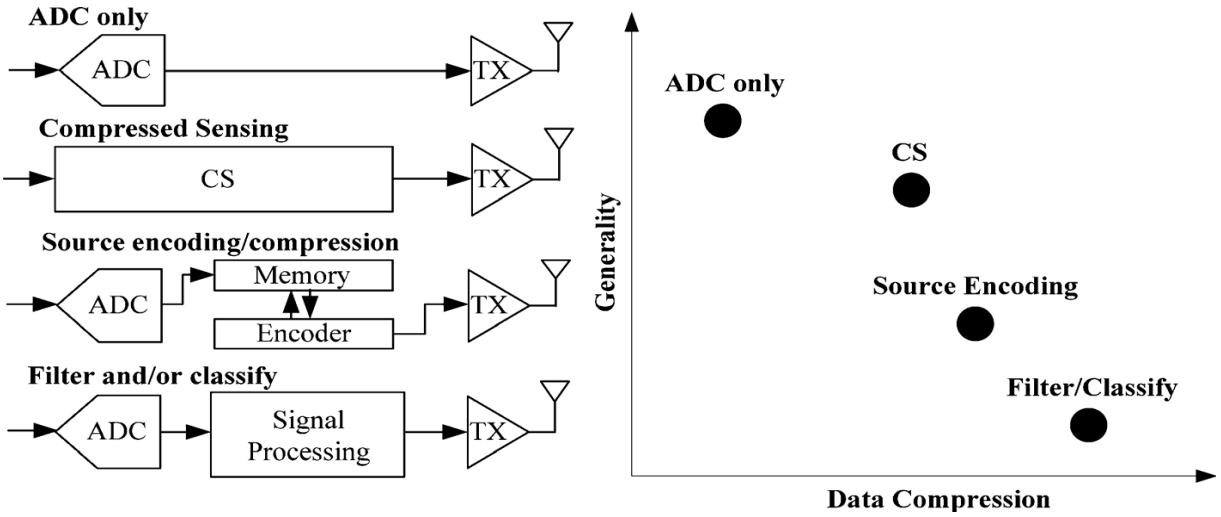


Figure 2: Relative compression approaches used in wireless sensors.

A. Basic Techniques Of Wireless Sensor Node

WSN consists of spatially distributed autonomous nodes that use sensors to monitor physical or environmental conditions. Each wireless node has four main sections including sensing unit, processing unit, communication unit and an energy supply unit. The wireless sensor nodes are usually deployed to acquire measurements such as temperature, pressure, flow, humidity, position and torque to the gateway. The gateway collects the measurement from each node and sends it over a wired connection, typically Ethernet, to a host controller. Wireless nodes in gateway sense information around their monitoring distance except the sink nodes in end layer that only get the information from other nodes and make decisions. The amount of information that should be processed in a gateway is huge which causes global traffic. The Embedded System promises to reduce the global traffic and to decrease data correlation.

B. Power Supply Unit

Power is a primary constraint in the wireless nodes and the power supply should provide power for sensing unit, communication unit, and processing unit. This fundamental power constraint further limits everything from data sensing rates and bandwidth, to node size, cost, security and weight. The power supply unit in most of the cases is a battery. The battery lifetime is related to the discharge rate or amount of current drawn. There is a focus on increasing the lifetimes of power supply through power management. This is all due to the fact that maintenance and replacement of power supply is expensive and difficult. Today, power management

technologies in WSNs are constantly evolving due to extensive research. The primary limiting factor for the lifetime of a wireless node is the energy supply. Each node must be designed to manage its local supply energy in order to maximize total network lifetime. A wireless node periodically wakes up to acquire and transmit data by powering and then it goes back to sleep mode to conserve energy.

C. Sensing Unit

WSNs consist of lots of sensors which measure pressure, temperature, humidity, flow, position to monitor physical. The sensors are deployed randomly in the certain area and are correlative. The wireless sensors are capable of sensing their environments, processing the information locally, and sending it to one or more collection points through a wireless link. There are some standards which govern the communication between the sensor nodes. The IEEE 1451 standard provides roles for wireless sensors to make it easier for different manufactures to develop sensors and interfaces to WSNs.

D. Processing Unit

The Processing unit consists of microcontroller or microprocessor, memory, interfaces, counters and timers. Regarding the application of WSNs, the processing unit has many types of microcontrollers or microprocessors from 4 to 64 bits. The 64-bit microcontrollers have three states or modes: sleep, idle, active modes. They support different power consumption in each mode. In the active mode, a clock is also still running, which can be used for scheduled wake ups, when the microcontroller switches to other modes. As a result, the consumption is decreased, and the battery lifetime is increased. The active mode consumption power is approximately 10 times more than sleep mode. Longer sleep mode is the best way to reduce power consumption of microcontrollers. One can anticipate longer sleep mode with CS since the CS decreases the number of information and consequently the sleep mode time will increase. Subsequently, the power consumption in microcontroller should be decreased if CS is used.

3. The Chosen Software

Multisim is a schematic capture and interactive simulation environment for analog and digital circuits. By wrapping the capabilities of SPICE simulation within a graphical interface, it is easier and quicker to simulate circuits. Multisim has a number of different analyses, ranging from transient to AC analysis, from Monte Carlo to Worst-Case. Multisim connects to layout tools such as Ultiboard and Mentor Graphics to physically prototype the circuit. LabVIEW is a graphical programming language, designed for rapid development of applications. It enables engineers to quickly connect to hardware, and acquire real measurements. By utilizing LabVIEW, engineers can graphically define algorithms to analyze measured data specific to the needs of the application. It is by unifying these two environments that both real and simulated measurements can be compared and analyzed, to improve the validation of physical circuits. This unification can be done through the Multisim Automation API. The API allows the automation and acquisition of Multisim simulation through a COM-based interface. The API lets you programmatically control a Multisim simulation without needing to view Multisim. Clients written in any COM-aware programming language, such as NI LabVIEW, can access Multisim through this interface, and leverage the simulation engine to acquire simulated measurements.

4. System Function and Structure

Data compression system receives the six-channel wave gate acquired data transmitted by AD acquisition card, which is processed through the digital down-conversion and its data format is two-way 16 bit fixed-point. After the six-channel pulse fix-point compression processing performed by the data compression system, its data format is converted to single-precision floating-point, then is transmitted to the PIC for further processing. The main parameters on data compression processing are as follows: Input format of digital down conversion: 16bit signed integer. Data format after data compression two-way, standard single-precision floating point. Frequency of AD down-convert signal acquisition: 70MHz IF, 30MHz bandwidth. Channels after pulse compression parallel processing: 6. Time requirements on single data compression processing 70us. Method of pulse compression processing: frequency domain approach. Speed of data transmission: 800MB/s.

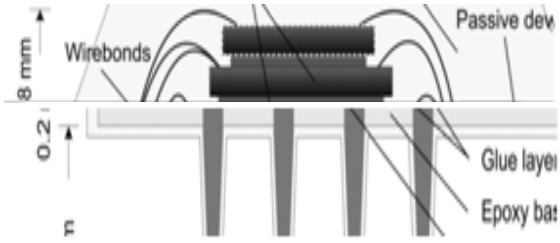


Figure 2: Conceptual representation of the 16-channel multi-chip interface.

5. Discussion

A. Modeling Results

In the case of the digital system, the model is relatively mature and there are few modeling assumptions so the predicted results correlate well with the measured results. For the analog system, however, there are some built-in assumptions to the model that will generally produce optimistic power numbers. For example, it is assumed that the circuit components perform ideally such that the integrator and mixer perform perfect accumulation and multiplication like their digital counterparts. In reality this will not be true, so when comparing the digital and analog systems at the same specifications, the resulting system performance will not be identical. For the power comparison in this work, the results favored the digital implementation despite the optimistic analog power estimate, but care should be taken to analyze these assumptions when the system specifications result in similar power performance.

B. Model Applicability

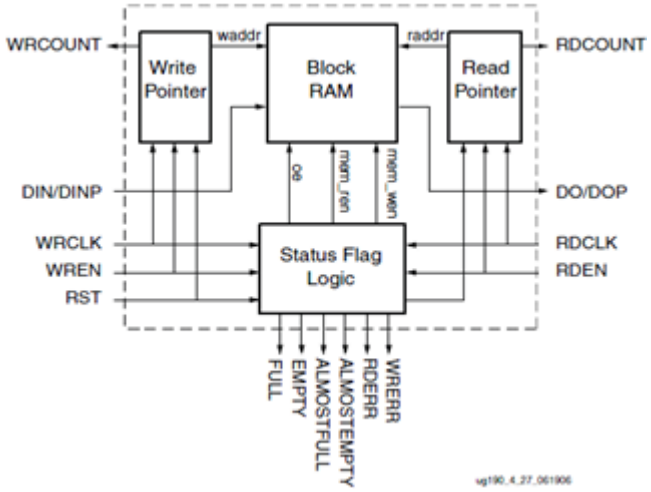
The inputs to the power modeling framework presented consist only of technology parameters, circuit performance specifications and system specifications. So to the extent that these inputs are well defined, the model is applicable to any application. One clear extension of the model is to analyze the power tradeoffs for AIC applications. AICs, which are identical to the analog system presented, have been proposed as a way to reduce the sampling frequencies of ADCs but it has never been clear if it is generally a more power efficient approach than an ADC alone.

C. Compression Performance and Cost

The measured results have shown compression performance that is on the same order of magnitude as previous feature extraction systems without requiring any decision making at the sensor node, while the energy-efficiency and power cost of the system is on par with or better than a custom feature extraction ASIC. However, since CS is performing data compression rather than any decision making, it is more appropriate to compare it to other compression/source coding schemes. For comparison, we limit this discussion to lossless compression alternatives since the quality of the recovered signal is known and independent of the signal type. This represents the coding efficiency that one might achieve with an infinite length Huffman code which is calculated as where is the probability mass function of , and represents the distribution of samples in the signal. This result is to be expected as the sample entropy does not take advantage of correlations between samples in the signal. Typically, the Lempel–Ziv–Welch (LZW) compression algorithm is more suitable for this purpose as it is more efficient at encoding repetitive data. The size of the minimum encoded output from the LZW algorithm is 2950 bits(295 10-bit code words) resulting in a coding efficiency of 2.95 bits per sample. So in this example, when compared to CS, a 6X penalty in transmission energy is paid to achieve lossless compression. For LZW to improve its coding efficiency, the block length (and input length) of the encoder must increase such that longer repetitions in the signal can be more efficiently encoded.18 For LZW, this requires a larger code dictionary and longer code sequence to be stored before transmission, which requires greater hardware cost. As seen in our power analysis, digital circuits for low bandwidth applications, such as wireless sensors, will often be leakage limited, so more storage implies more power. Thus, for any alternative compression scheme to be competitive with CS in terms of power, the storage requirements must be on the order of 1000 flip-flops19 or less. In the case of LZW, the example just described consumes only 3 k storage elements for the coded output, but the corresponding dictionary needed to generate that output code requires an 11 k memory20 where the storage requirements for both the output code and dictionary increase as higher compression is desired. Even without accounting for differences in computational complexity (which favors CS), the CS compression system, though lossy, offers 6X higher compression at over 10X lower implementation (storage/power) cost.

D. The Design of Data Buffer Module

In the data compression system, data buffer module is used mainly for receiving the data acquisition after down converter transmitted by ADC board, after meeting the data requirements on a data compression, the data waiting to receive is transmitted to the pulse compression module for processing. In addition, a buffer is required for the data after pulse compression processing; the asynchronous FIFO is used to achieve the data buffer design in this design. It provides two memory structures: Distributed memory architecture and block memory structure. Distributed Memory (Distributed Select RAM) is achieved by the CLB's lookup table (LUT). Block memory (Block RAM) is a special memory module, each 18Kb; number varies as the device size, which can be configured for single or dual port Block RAM. Compared with the distributed storage structure, block storage architecture can achieve higher clock speed; therefore, we used block memory to achieve the asynchronous FIFO in the design. Top-Level View of FIFO in Block RAM as shown in
Fig 3



6. Simulation Results

Digital block was partitioned into hierarchy modules firstly, the RTL coding of sub-modules have been simulated in Multisim10.1. The simulation result as shown in Fig4. The last two line waveforms are the real part and imaginary part of the data after data compression. So, the functional simulation results in the MultiSim 10.1 verify the design and the code before downloading the program, which is the necessary step in the design to avoid the hardware damage.

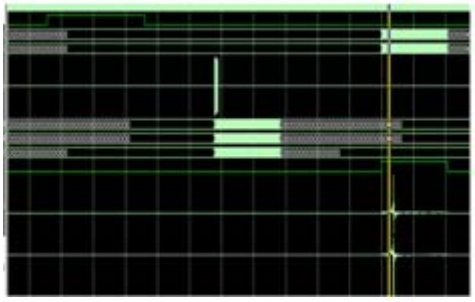


Figure 4:.Simulation results

7. Conclusion

This paper introduces the software design of the signal-processing in the multichannel data compression system. We develop the program and, use MultiSim 10.1 for the function simulation. In future scope of this paper it was used Broad range of application agriculture, health care. Where ever using the multi sensor node to collect raw analog/digital data in wireless.

8. Acknowledgment

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