Design of Modified Parallel Prefix Knowles Adder

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Abstract:-*Parallel Prefix Adders plays a prominent role in Digital Combinational Circuits . The basic function of adder in ALU is addition that is also used in Multipliers which results in decrease or increase of Delay that depends on the architecture of adder. Area and power are another important factors which really makes the adder effective The high performance digital adderswith reduced area and low power consumption is an important design constraint for modern advanced processors . So, low power adders are also a need for today's VLSI industry. This Paper discusses the design of novel design of 16 bit Parallel Prefix adder. This adder is a mixture of two types of adders i.e Brent Kung and Knowles adder. At last there is comparison of 8 and 16 bit Knowles , 8 and 16 bit Modified knowles adder that is our Proposed design our design shows better performance from that of parallel prefix knowles and kogge stone adder in terms of power, area and Combinational path delay.*

Keywords: Modified Knowles adder, carry look ahead adder, Knowles adder, Parallel Prefix adder

1. Introduction

In Modern digital world Arithmetic Operations are widely used in VLSI Industry. Addition is the basic Operation used in all multiplication, subtraction & division or we say that these operations derived from Addition. That's why it is an integral of ALU. The Performance goal for today's modern VLSI Industry is reduced area & Low Power adders. A parallel Prefix adder uses Carry Look ahead adder carries Propagation and generation and also used for addition at the last stage. So, Let us first discuss what the Carry Look ahead is.

2. Carry Look ahead adder

A carry-look ahead adder (CLA) is a type of adder used in digital logic. It improves speed by reducing the amount of time required to determine carry bits The carry-lookahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits. The Kogge-Stone adder and Brent-Kung adder are examples of this type of adder. In order to implement the carry look ahead adder, we need to define the propagation bit(P) and generation bit(G) of each input signal in equations:

$P_i = A_i + B_i$--(i)$G_i = A_i + B$--(ii)
$C_{i+1} = G_i + P_i . C_i$ --(iii)

3. Knowles adder

The parallel-prefix tree adders are more favourable in terms of speed due to thecomplexity O(log2N) delay (Kogge stone) through the carry path compared to that of other adders. This is similar to kogge stone adder except in Last stage wiring complexity is reduced to half . But it double the Loading. Kogge-Stone adder design is the most straightforward, and also it has one of the shortest critical paths of all tree adders. The drawback with the Kogge-Stone adder implementation is the large area consumption and the

more complex routing (Fan-Out) of interconnects. Black boxes are BC and grey cells are GC that cannot be removed, because they are required for carry propagation and other calculations.
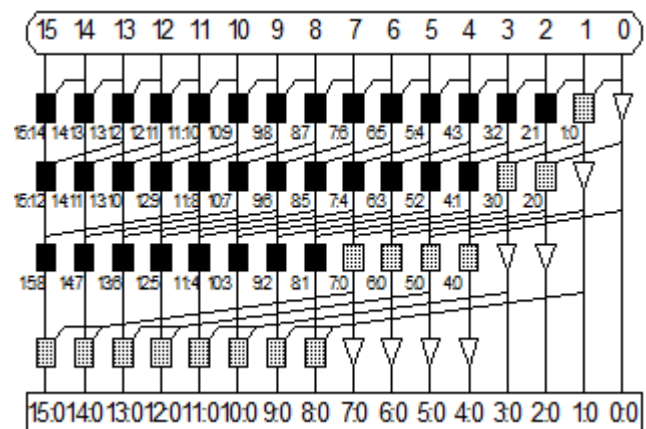

Figure 1: 16 Bit Knowles adder

Fig. 1 Shows the 16 bit knowles adder So, we need an adder in which we reduce the area . for this we have reduce the no. of cells so, area will reduce that will also reduce the power. Kogge-Stone is one of the fastest type of parallel prefix adders . So, what will happen If wereduce the fanout of knowles adder and also reduce the cells speed will increase and area and Power will drastically decreased . Let us see how it will happen.

4. Modified Knowles adder

In this adder we take the First stage of Brent kung adder and rest of stages remains the same as Kogge stone adder . Fig 2 Shows the architecture brent Kung adder. PG is propagate and generate cells , BC are Black cells and C0-C15 are carries also known as Black cells. Blue Circles indicates sum. In Kogge-stone adder, carries are generated fast by computing them in parallel at the cost of increased area and large loading in case of Knowles adder. (GC) Grey cells are

required for computation of generate bit in final stage and thus cannot be removed. Black cells are the only redundant cells in Parallel Prefix adders. Thus all changes which are going to be done have to be done in perspective of speed. The last stage gives us a much better understanding of the decrease in fanout to decrease the loading and If we compared the knowles adder with modified Knowles adder , Fig 3 shows the Modified Knowles adder First stage is the Brent kung stage and resr are same as the Knowles adder stages .We mix the two Adders to get the best results , Also Brent Kung has more logic levels than that of knowles adder. That's why It was the worst design so far as compared to all other parallell Prefix adders. But we are interested only in stage one of brent kung (from 1:0 to 15:14), we will make next stages by using the logic Knowles adder itself.

4.1 Gray cell

The gray cell takes two pairs of generate and propagate signals (Gi, Pi) and (Gj, Pj) as inputs. Computesa generate signal "G"
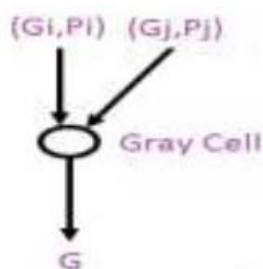as output
$Gi,j = Gi + (Pi . Gj)$(iv)

Figure 2: Block diagram of GC

4.2 BC block

The black cell takes two pairs of generate and propagate signals (gi, pi) and (gj, pj) as input.
Computes a pair of generate and propagate signals (g, p) as output
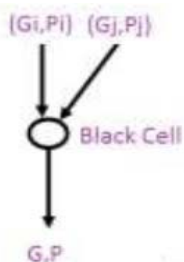$Gi.j = Gi + (Pi .Gj)$(v)
$Pi.j = Pi .Pj$(vi)

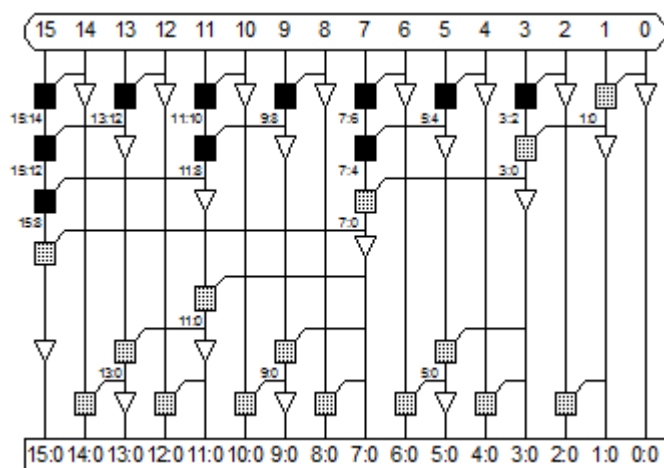**Figure 3:** Block diagram of Black Cell
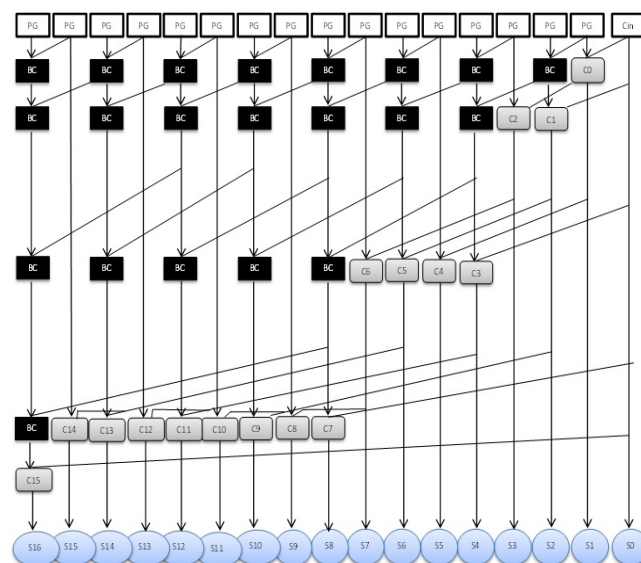

Figure 4: 16 bit Brent Kung adder


Figure 5: 16 bit Modified knowles adder

Then an improvement 7.61 % Combinational path delay is also achievedFig 3.Shows Modified Parallel Prefix Knowles adder. The main purpose of adder is to speed up the addition of partial products generated during multiplication operation. Hence improving the speed by reduction in area is the main area of research in VLSI system design.The main advantage using Modified Knowles adder design is that it reduces the number of Black cells bycombining the architecture of Knowles adderand Brent Kung,Infactthe operation remains the same as that of Knowles adder.

5. Results

Results are obtained using Xilinx 14.2 tool and Cadence RTL Compiler. Path delay (ns) is calculated automatically using synthesis process in Xilinx Tool, Area and Power are Calculated using Cadence RTL Compiler Tool.

Table 1: Comparison of Knowles and Modified Knowles adder

Parallel Prefix Adders	Area	Power(nw)	Path delay(ns)
16 bit Knowles adder	414.893	9993.106	14.452
16 bit Modified Knowles adder	340.805	8886.989	13.369
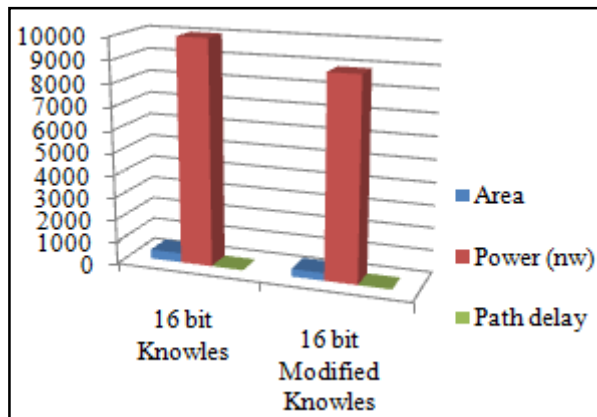
6. Conclusion

This paper presents an innovative way of modifying the already existing Knowlesadder by removing the Black-cell for increasing the speed of execution. The design originates from theprinciple of removing the black cells by Joining two types of adders .The above design has a delay , area and power much less than the architectures that it is being compared with. There is a reduction in Combinational Path delay by 7.61% to that of normal Knowles adder. So parallel prefix adders of this type are the best choice in many VLSI applications where power, area and also speed is the main constraint.

7. Future Scope

Parallel-prefix structure is attractive for adders because of its logarithmic delay. The influence of design trade-offs can be easily observed from adder designs. Considering all the possibilities, there are still plenty to explore for adder design. Current adder design is made by combination of Brent Kung and kogge stone adder. We can check some more combinations by using some other Prefix adders.

As an attempt to develop arithmetic architecture level optimizations techniques for low-power Parallel Prefix Adder Design, The research presented in this dissertation has achieved better results. However several future research directions are also possible in this area. Higher bit i.e. 32 bit and so on adder can be simulated and observe the variation in parameters as power, area and delay.

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