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Analysis of Clock Gating For Dynamic Power Reduction in JK Flip Flop with Transmission Gate

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Abstract: ***In this paper clock gating technique along with a comparator circuit is presented for low power VLSI (very large scale integration) circuit design. The rapid increase in the number of transistors on chips enabled a dramatic increase in the performance of computing systems. However, the performance improvement has been accompanied by an increase in power dissipation; thus requiring more expensive packaging and cooling technology. Reducing power dissipation is one of the most principle subjects in VLSI design today. Clock gating is a technique to reduce clock power with the help of transmission gate. In this paper 3bit JK flip flop is designed using transmission gate. 3 bit JK flip-flop is constructed by connecting three JK flip-flops in series i.e. output of first JK flip-flop is fed as input of second JK flip-flop and the output of second JK flip-flop is fed as input of third JK flip-flop. Transmission gate has three input, called source, n-gate, and p-gate; and it has one output called drain. The transmission gate is simply the combination of two complementary transistors. Also a comparator circuit is added between input and output of JK flip flop. Simulation is perform by the Tanner tool and the experimental result shows that the clock gating technique is along with comparator circuit is able to reduce average power consumption. Average power is calculated in both the cases i.e. conventional JK flip-flop circuit and proposed JK flip-flop circuit. It is observed that approximately 16% of dynamic power is saved.***

Keywords: Transmission gate, Static power, Dynamic Power, JK flip flop, Clock gating etc**.**

1. Introduction

The Paper describes our experience with the transmission gate clock gating for dynamic power reduction in JK flip flop. Simulation is perform by the Tanner tool and the experimental result shows that the clock gating technique is along with comparator circuit is able to reduce average power consumption.

1.1 Clock Gating

Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Reducing power consumption in very large scale integrated circuits (VLSI) design has become an interesting research area. Most of the portable devices available in the market are battery driven. These devices impose tight constraint on the power dissipation. Reducing power consumption in such devices improves battery life significantly. Due to lesser advancement in battery technology, low power design has become more challenging research area. Power consumed in a digital circuit is of two types.

1) Static power
2) Dynamic power.

Average power dissipated in a digital circuit is given as.

P average = P dynamic + P short-circuit + P leakage + P static

P average is the average power dissipation, P dynamic is the dynamic power dissipation due to switching of transistors, P short-circuit is the short-circuit current power dissipation when there is a direct current path from power supply down to ground , P leakage is the power dissipation due to leakage currents, P static and is the static power dissipation.

1) **Static Power**
   Static power is the power dissipated by a gate when it is inactive or idle. Ideally, CMOS (Complementary Metal Oxide Semiconductor) circuits dissipate no static (DC) power since in the steady state there is no direct path from Vdd to ground.
2) **Dynamic Power**
   Dynamic power is the power dissipated during active state due to switching activity of input signal. In other words, dynamic power dissipation is caused by the charging.
   Dynamic power dissipation in a circuit is given as.
   PD = α CL VDD2f.
   Where α is the switching activity, f is the operation frequency, CL is the load capacitance, VDD is the supply voltage.

1.2 Transmission Gates

CMOS TG consists of one nMOS and one pMOS transistor connected in parallel is shown in figure 1 . CMOS TG operates as a bidirectional switch between the nodes A and B which is controlled by signal C. If C is high, both the transistors are turned on and provide a low resistance current path between the nodes A & B. If C is low, both the transistors are turned off and path between the nodes A & B will be an open circuit, called high-impedance state.

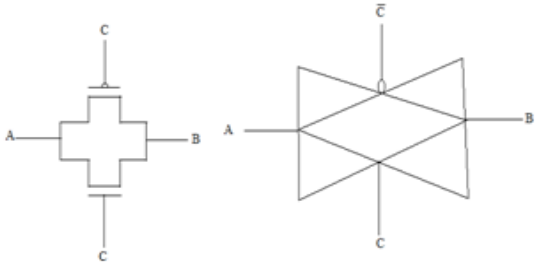

Figure1: Transmission Gates

CMOS Transmission Gates can be used in logic design; a savings in transistors is often realized.

1.3 Logics

In the proposed design the proposed JK lip is intent to design by using D Flip Flop, it can simply be realized by having some extra logic on input (D) of D Flip Flop.

Table 1: JK Logic Table

J	K	Qnext
0	0	Q(Hold)
0	1	0(Reset)
1	0	1(Set)
1	1	Qbar(Toggle)

The proposed design is intent to use a comparator circuit at the between input and output of JK Flip Flop, which can be employed by using a xor gate. As the xor gate properties are:

Table 2: XOR Logic Table

D	Q	OUT
0	0	0
0	1	1
1	0	1
1	1	0

The reason behind using xor in the design is that it'll create high output only when either:
1. Input (D) is High and Output is Low.
2. Input (D) is Low Output is High.

2. Previous Research Work Describing Techniques

2.1 Clock Gating Technique

The clock gating is intent to implemented by using ANDing of comparator output signal and clock of the design, hence producing asserting gated clock high when both the signals are high.

Clock power is a major component of power mainly because the clock is fed to most of the circuit blocks, and the clock switches every cycle. Thus the total clock power is a substantial component of total power dissipation in a digital circuit. Clock-gating is a well-known technique to reduce clock power. By clock gating technique, clock to an idle portion is disabled, thus avoiding power dissipation due to unnecessary charging and discharging of the unused circuit. In clock gating clock is selectively stopped for a portion of circuit which is not performing any active computation. This is done by using a signal from the environment. An example of gated clock is shown in figure.

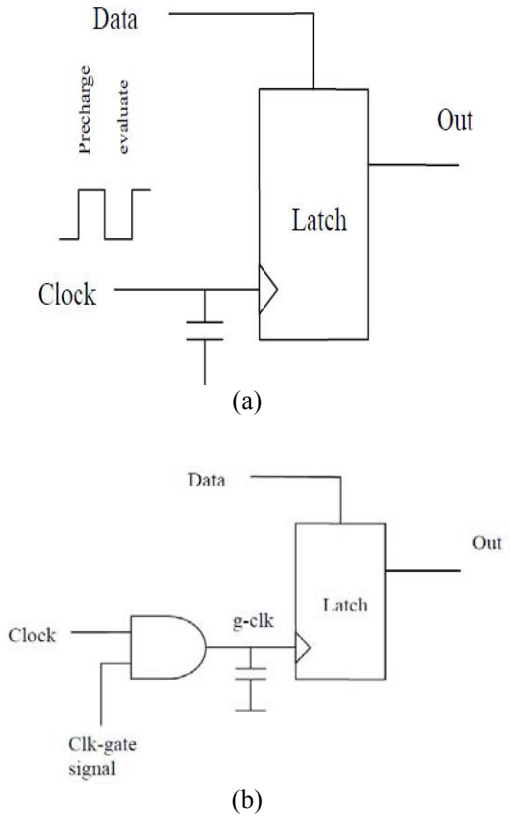

Figure 2: (a) synchronous latch without clock gating, (b) gated clock implementation in latch

3. Proposed Design Clock Gating Technique

The proposed circuitries intend to reduce power consumption using transmission gates in the JK flip flop circuit. Simulation is performed with the help of Tanner Tool version 13.0.These proposed designs consist of a JK flip-flop, a comparator circuit and a clock gating circuit. The proposed JK flip-flop is intent to design by using D Flip Flop, it is simply be realized by having some extra logic on input (D) of D Flip Flop. The proposed design is also intent to use a comparator circuit at the between input and output of JK Flip Flop, which is employed by using a xor gate. The clock gating is intent to implemented by using ANDing of comparator output signal and clock of the design, hence producing asserting gated clock high when both the signals are high.

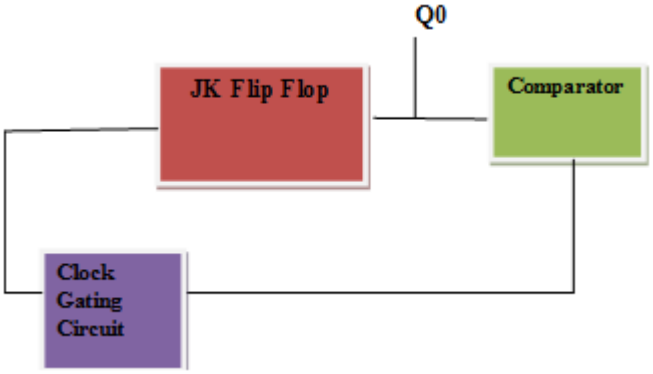

Figure 3: Block representation of proposed design

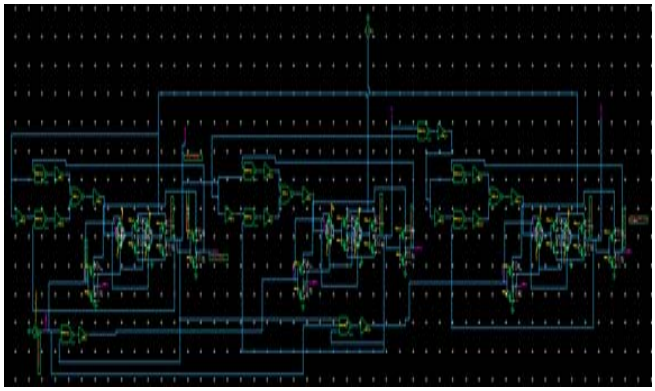

Figure 4: Conventional JK circuit

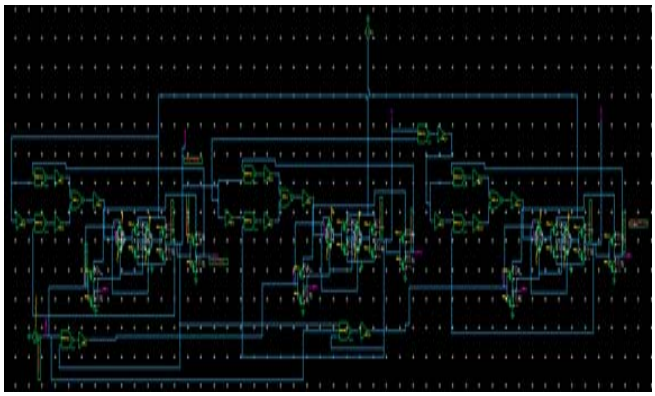

Figure 5: Proposed circuit

4. Simulation Waveform

Figure 6: Conventional JK waveform

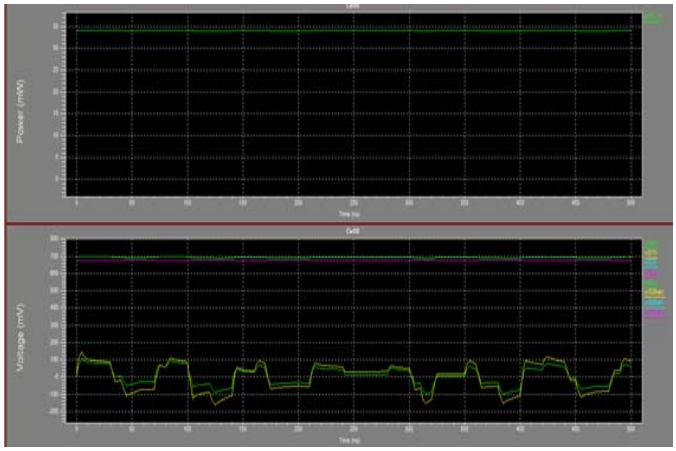

Figure 7: Proposed JK waveform

5. Power Consumption

Table 3: Power comparison

Logic	Average Power
Conventional JK	4.055884e-002 watts
Proposed JK	3.405143e-002 watts

Clearly we can see the change in power consumption by both the circuits. Using the proposed circuitry we can reduce about 16% power consumption which is a remarkable achievement now days.

6. Conclusion

Leakage power is actually consumed when a device is both static and switching, but generally the main concern with leakage power is when the device is in its inactive state. Dynamic power consists of switching power, consumed while charging and discharging the loads on a device, and an external power (also referred to as short circuit power), consumed internal to the device while it is changing state. Various techniques have been developed to reduce both dynamic and leakage power. One of the techniques is proposed in the paper by adding clock gating technique along with comparator circuit in the JK flip-flop circuit. The average power consumed in both the circuit i.e. conventional JK flip-flop and proposed JK flip-flop clearly shows that the average power consumed in case of proposed JK flip-flop is much lesser than the conventional JK flip-flop.

7. Future Scope

In this proposed design further consumed power and energy by using additional gates and other technique. Many techniques are developed in electronics field to reduce the size and power.

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