Implementation of a Pacemaker for Biomedical Application

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Abstract: *In this project work A state machine approach has been followed to design and implement a single and dual chamber pacemaker in response to different heart beats from 35bpm-125bpm. The heart of the pacemaker system rests in the pulse generator which forms the major portion of the project. It has been developed using Verilog and implemented in hardware using FPGA. In the FSM, first an input event is detected. Once this input is detected a timer is set which will be the time between heartbeats, thus giving 35-125 heartbeats per minute. This pacemaker responses only when the QRS wave is low or high in compared to normal ECG wave. The designing and verification is done through verilog on Xilinx 14.1. Also, ECG signal is generated in modelsim 10.1b. The pacemaker response is verified with various heart beats from 35-125bpm.*

Keywords: ECG, pacemaker, single chamber pacemaker, dual chamber pacemaker, verilog.

1. Introduction

Pacemakers were first introduced in the 1950s, with only few transistor used in the device. Technology has advanced greatly and there are over tens of millions of transistor in today's implantable pacemaker system. A cardiac pacemaker is used to treat bradycardia (a heart rate that is too slow) and tachycardia(a heart rate that is too slow). This pacemaker monitor the heart's rate (how fast it beats) and rhythm (the pattern in which it beats), and provides electrical simulation when the heart does not beat or beats too slowly or too high.

The paper briefly introduces the general aspects of single and dual chamber pacemaker Structure and functions. Generating ECG signal in Matlab. Extracting these signal coefficients for different heart beat from 35-125bpm and storing in LUT and generating this signal in modelsim. This designed pacemaker works only when the QRS wave is low or high in compared to normal ECG wave. Depending upon the heart beats from 35-125bpm with ecg signal the single and dual chamber chambers will turn on or off.

2. Implementation

2.1 ECG signal generation

ECG is used to measure the heart's electrical conduction system. It picks up electrical impulses generated by the polarization and depolarization of cardiac tissue and translates into a waveform. The waveform is then used to measure the heart rate. It records any problems with the heart's rhythm, and the conduction of the heart beat through the heart which may be affected by underlying heart disease.
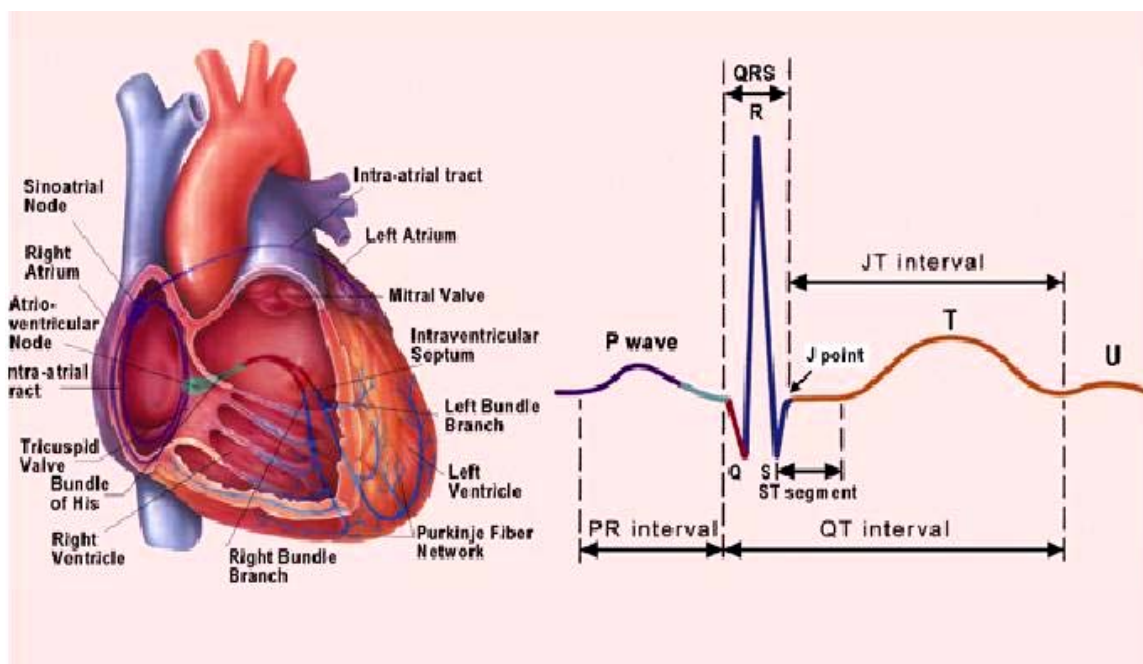

Figure 2.1: The ECG signal generation

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ECG signal can be generated using Fourier series which satisfies dirichlet's condition. Any periodic functions which satisfy dirichlet's condition can be expressed as a series of scaled magnitudes of sin and cos terms of frequencies which occur as a multiple of fundamental frequency.

ECG signal is periodic with fundamental frequency determined by the heartbeat. It also satisfies the dirichlet's conditions:
- Single valued and finite in the given interval
- Absolutely integrable
- Finite number of maxima and minima between finite intervals
- It has finite number of discontinuities

Hence Fourier series can be used for representing ECG signal. This signal can be generated using matlab for different heart beats from 35-125bpm. These coefficients are extracted and stored in look up table (LUT). For these values verilog code has been developed to extract ECG waveform
ECG specification: ECG: 0-100hz
- ECG amplitude range=0.05-3V
- Heart amplitude~0.5mv
- Normal heart beat range= 60-90 bpm
- Bradycardia heart beat range=below 60bpm
- Tachycardia heart beat range= above 95bpm
- P duration < 0.12 sec
- P amplitude < 0.25 mv
- QRS duration ≤ 0.11sec
- Qrs wave amplitude <2.4mV
- PR interval=0.12 - 0.20 sec
- Qrs wave duration=0.06 - 0.10 sec
- S wave amplitude<0.35mv
- T wave amplitude <=0.35mV

Table 1: ECG signal output for different heart beats

Heart beats (8bit)	clk	rst	validin	Sensor_out
35	1	1	0	0
35-55	1	0	1	0
65-85	1	0	1	1
95-125	1	0	1	0

2.2. Single Chamber Pacemaker

A single chamber pacemaker is one which only one of the two chambers of the heart atrium or ventricles is paced, since ventricle have stronger muscle and they have to pump the blood to longer distance compared to atria i.e. sensing and pacing is done at ventricle. The wires in a single-chamber pacemaker carry pulses between the right ventricle (the lower right chamber of your heart) and the generator.
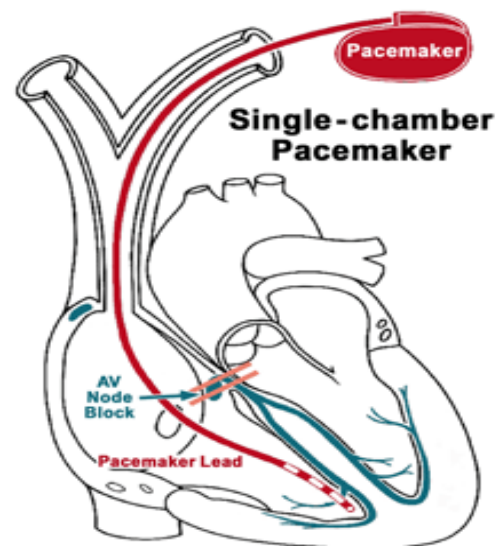

Figure 2.2: Single chamber pacemakers

2.3 State diagram for single chamber pacemaker

The state machine designed for this pacemaker consists of three states: ResetTimer, Wait and Pace. The system gets the input from the ECG signal through the sensor if presence of QRS wave is sensed or not. Depending on 'S' it stays in the wait state or goes to the pace state. When normal QRS wave sensed then the pacemaker resets the timer.
So the general flow of a complete cycle of the pacemaker goes in the following path:
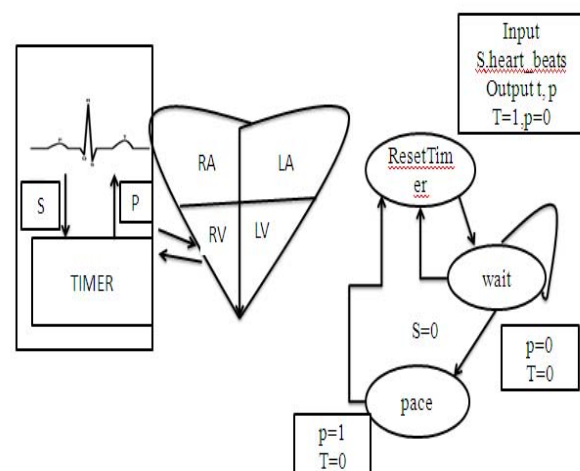
Reset Timer ⟶ Wait ⟶ Pace

Inputs:
S: sensing parameter: 1 if normal QRS wave is detected else 0.
Heart_beats: the number of heart beats per minute , 35-55bpm, heart_beats=1; 65-85bpm, heart_beats=0; 95-125bpm, heart_beats=1
Outputs:
T: output to timer: 1 if timer is to be reset.
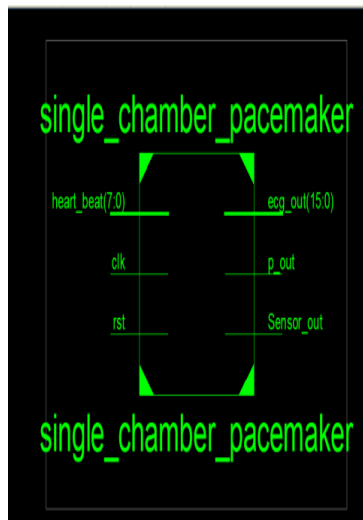**P**: output to heart: 1 if pacing needs to be done.

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Figure 2.3: State diagram of single chamber pacemaker

Table 2: State table of single chamber pacemaker

state	function	input	input	output	output
		S	Heart_beats	P	T
A	Wait	0	0	0	0
B	Pace	0	1	1	0
C	Reset	1	0	0	1
	Timer	1	1	0	1

2.2. Dual Chamber Pacemaker

A pacemaker with pacing electrodes in both the right atrium and the right ventricle, which helps maintain the physiological relationship between atrial and ventricular contraction, and allows the paced heart to follow the increase in sinus rate which occurs during exercise. The wires in a dual-chamber pacemaker carry pulses between the right atrium (the upper right chamber of your heart) and the right ventricle and the generator. The pulses help coordinate the timing of these two chambers contractions. Dual-chamber pacemakers tend to prevent more subsequent heart problems than single-chamber ventricular pacemakers.
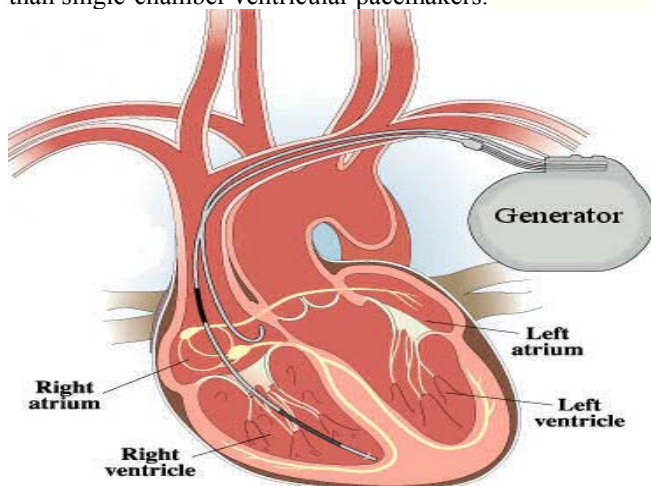
Figure 2.4: Dual chamber pacemaker

This is an extension of the single chamber to dual chamber pacemaker. The basic working principle is the same as single chamber pacemaker. Just that after the pacing of atrium, the state changes to the 'Reset Timer' state of the ventricle and not the 'Reset Timer' state of the atrium. So the general flow

of a complete cycle of the pacemaker goes in the following path:

Reset Timer A ⟶ Wait A ⟶ Pace A
Reset Timer V ⟶ Wait V ⟶ Pace V.

Then the process continues in a cyclic manner again.
The following is the state diagram.
The inputs and outputs hold the same significance; 'a' suffix stands for atria, and 'v'Suffix sands for ventricle.

Inputs:
sV: sensing parameter: 1 if contraction is sensed in the ventricle.
Heart_beats: the number of heart beats per minute , 35-55bpm, heart_beats=1; 65-85bpm, heart_beats=0; 95-125bpm, heart_beats=1
Outputs:
tV: output to timer: 1 if timer for the ventricle is to be reset.
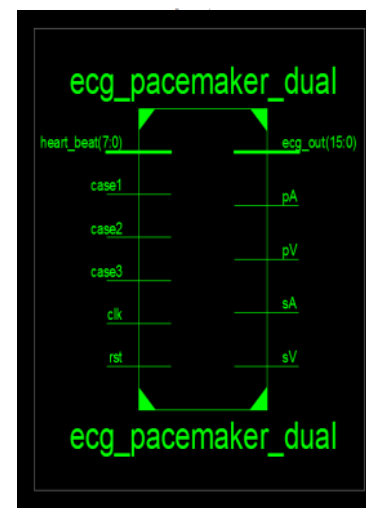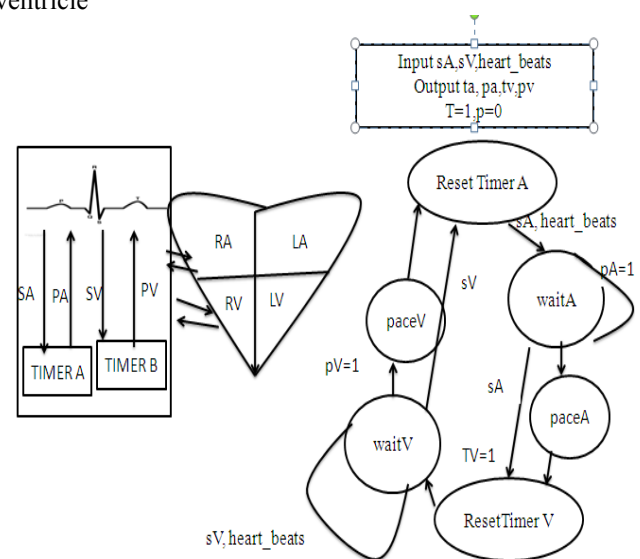pV: output to heart : 1 if pacing needs to be done in the ventricle

**Figure 2.5:** State diagram of dual chamber pacemaker

Table 3: State table of dual chamber pacemaker

| State	Function	i/p	i/p	o/p	o/p	o/p	o/p	o/p
		sA	Heart_beat	sV	pA	pV	tA	tV
A	waitA	0	0	x	0	0	0	0
B	paceA	0	1	x	1	0	0	0
C	ResetA	1	0	x	0	0	1	0
	TimerA	1	1	x	0	0	1	0
D	waitA	x	0	0	0	0	0	0
E	paceA	x	1	0	0	1	0	0
F	ResetA	x	0	1	0	1	0	0
	TimerA	x	1	1	0	0	0	1

3. Experimental Results

The pacemaker designed in Verilog HDL and verified its Functionality. The syntax of the RTL design is checked using Xilinx tool. The pacemaker design is first simulated in ModelSim, shown in below figure. The design is verified both at a top level. The design has been Synthesized targeting Xilinx FPGA spartan3A (XCS200A -5fg256) device. The device utilization of both the pacemaker is shown in Table-I. The timing delay is also calculated for both the pacemakers, which shows that the single chamber pacemaker is consuming.
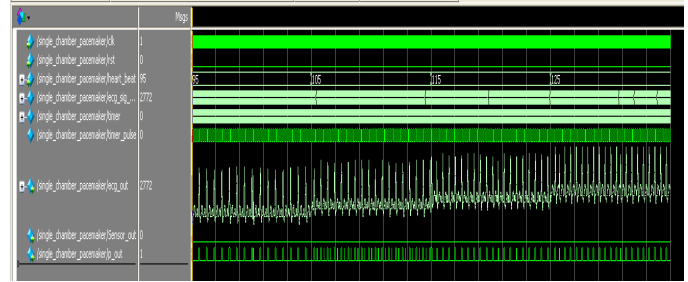
3.1(A) Bradycardia: rst=0, heart_beat= 35-55 sensor_out=0, pacemaker_out=1.
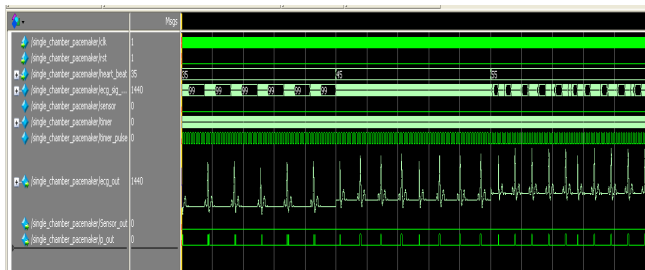
Figure 3.1(A): Simulation Results of Single chamber pacemaker

3.1(B) Normal heart beat: rst=0, heart_beat= 65-85 sensor_out=1, pacemaker_out=0.
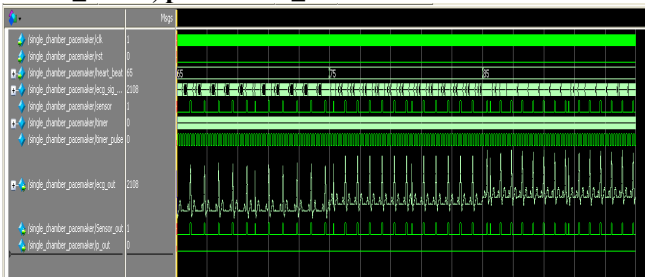
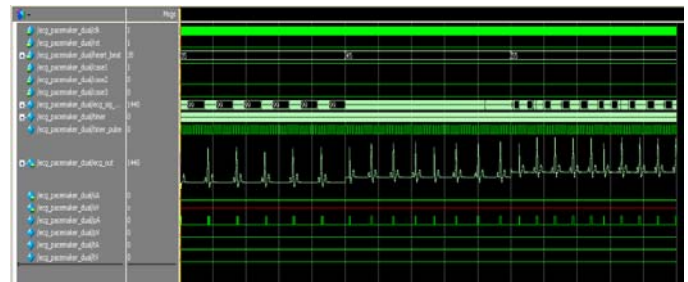**Figure 3.1(B):** Simulation Results of Single chamber pacemaker

3.1(C) Tachycardia: rst=0, heart_beat= 95-125, sensor_out=0, pacemaker_out=1.

Figure 3.1(C): Simulation Results of Single chamber pacemaker

3.2 Dual chamber simulation results

3.2(A) CASE 1: sA=1/0, sV=x , pA=1/0, pV=0
(a) Bradycardia: Rst=0, heart_beat=35-55bpm, sA=0, pA=1, pV=0.

Figure 3.21: Simulation Results of dual chamber pacemaker

(b) Normal Heart beats: Rst=0, heart_beat=65-85bpm, sA=1, pA=0,pV=0.

Figure 3.22: Simulation Results of dual chamber pacemaker

Device utilization	Available	Single chamber pacemaker		Dual chamber pacemaker	
		Used	Utilization	Used	Utilization
Number of Slices	1792	1715	95%	1685	91%
`Number of Slice Flip Flops	3584	14	0%	29	0%
Number of 4 Input LUTs	3584	3202	89%	3152	86%
Number of Bonded IOBs	68	28	41%	31	46%
Number of GCLKs	24	1	4%	3	8%

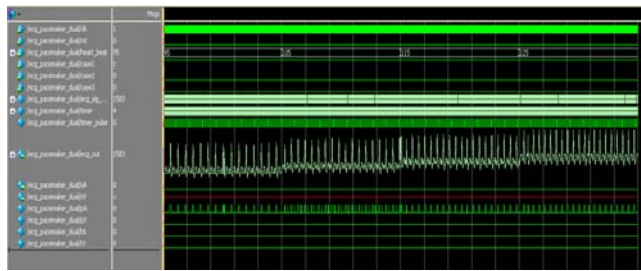*(c) Tachycardia:* Rst=0, heart_beat=95-125bpm, sA=0, pA=1,pV=0.

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Figure 3.23: Simulation Results of dual chamber pacemaker

3.2(B) CASE 2: sA=x, sV=1/0 , pA=0, pV=1/0

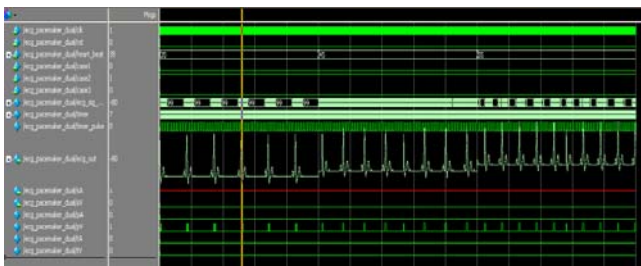*(a) Bradycardia: :* Rst=0, heart_beat=35-55bpm, sV=0, pA=0,pV=1.

Figure 3.24: Simulation Results of dual chamber pacemaker

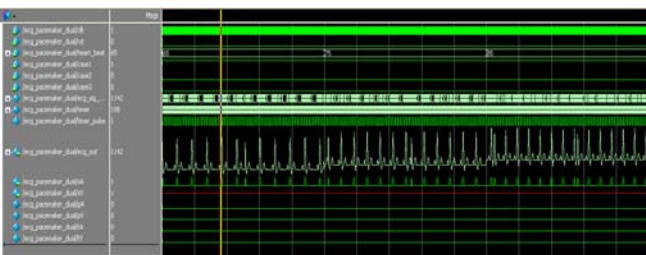*(b) Normal Heart beat:* heart_beat=65-85bpm pA=0, pV=0,sA=x, sV= 1, pA=0, pV =1.

Figure 3.25: Simulation Results of dual chamber pacemaker

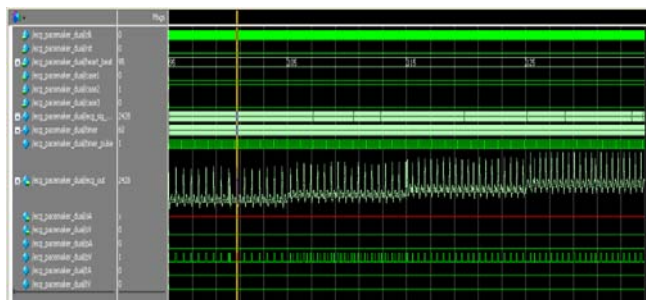*(c) Tachycardia:* Rst=0, heart_beat=95-125bpm, sV=0, pA=0,pV=1.

Figure 3.26: Simulation Results of dual chamber pacemaker

3.3 Device utilization of single and dual chamber pacemaker

3.4 Timing analysis of single and dual chamber pacemaker

Time & Frequency Analysis	Single Chamber Pacemaker	Dual Chamber Pacemaker
Minimum Period	3.867ns	3.842ns
Maximum Frequency	258.632mhz	260.276mhz
Minimum Input Arrival Time Before Clock	2.109ns	12.309ns
Maximum Output Required Time After Clock	21.241ns	15.225ns

3.5 Power analysis of single and dual chamber pacemaker

Supply Power	Single Chamber Pacemaker	Dual Chamber Pacemaker
Dynamic	0.001	0.004
Quiesent	0.022	0.021
Total	0.023	0.025

4. Conclusion

The single and dual chamber pacemaker is designed in verilog-HDL. The Simulation is done with Modelsim simulator and also implemented on Xilinx FPGA Spartan 3A(XC3S200A-5FG256).The Simulation & implementation results show that the designed pacemaker is working properly with all the heart beats from 35-125bpm.

5. Future Scope

Single and dual chamber pacemaker can be implemented to verify various modes like VVI mode, DDI mode and DDTR mode.

6. Acknowledgement

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