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Efficient Implementation of MIMO using OFDM Applications

M. Arun Kumar

Assistant Professor, Department Of ECE, Karpagam College of Engineering, Coimbatore, India

Abstract: ***Multiple Input Multiple Output Orthogonal Frequency Division Multiplexing (MIMO-OFDM) technology is an attractive transmission technique for wireless communication systems with multiple antennas at receiver and transmitter. The reliability of Data rate and diversity can be increased along with the stability for multi-path signals. The efficient implementation of a Low-Power 64-point Pipeline FFT/IFFT processor adopting a single-path delay. To achieve a ROM-less FFT/IFFT processor, thus less power is consumed using the complex multiplier reconfigurable and bit-parallel multipliers. Based Header channel estimation with maximum likelihood algorithm is chosen in consideration of hardware feature as well as communication theory. Simple logic is used in Pipeline architecture includes one adder and channel memories without redundancy. Can be reduced the complexity from O (n2) to O (1) it saves 43 percent of the hardware resources and achieves a better performance in the architecture.***

Keywords: MIMO-OFDM, FFT/IFFT, FPGA, Channel Estimation

1. Introduction

The growing demand for high broadband access high rate of transmission system capacity, and motivates researches to search a technology new, resulting in OFDM–MIMO technique. The OFDM- MIMO advantages are that it uses bandwidth more efficiently without the power is increased and the symbol interference (ISI) effect and effects of multi-path. High delay is caused by using a OFDM approach for spread channels or high data rate with equalizers of low complexity. Therefore OFDM- MIMO has physical layer of the most promising schemes in the fourth generation wireless systems communication. Cooley and Turkey proposed the Fast Fourier Transform (FFT) to efficiently reduce the complexity of time. For hardware implementation, various FFT processors have been proposed.

In future wireless communications system are designed to increase the efficiency and to improve reliability. The receiver provides diversity with (ideally independent) replicas of the transmitted signal and is therefore a powerful means to combat fading and interference and the improve reliability link. Time diversity are Common forms of diversity (due to Doppler spread) and frequency diversity (due to spread delay).The use of spatial in recent years (oran antenna) diversity can be provided without loss antennas on the receive side of a wireless system.

The Fast Fourier Transform (FFT) was proposed by Cooley and Turkey to efficiently reduce the complexity of time. Various FFT processors have been proposed for hardware implementation. These implementations can be mainly classified into memory-based and pipeline styles architecture. The Memory-based architecture is adopted widely to design an FFT processor, also known as the processing element with single approach. This style of design is composed of a main processing elements and several units of memory, thus the hardware cost and the power consumption are both lower than the other architecture style.

The style of architecture has latency is high, low throughput. The Pipeline architecture style can get rid off the disadvantages the cost of an acceptable hardware. Generally, the pipeline FFT processors have two popular types of design. The architecture uses pipeline architecture single-path delay feedback (SDF) and the other uses pipeline architecture with multiple-path delay commutate or (MDC). The single- path delay feedback (SDF) pipeline FFT is good in its requiring less memory space and its multiplication computation utilization being less than 50%, easy to design the control unit. Such implementations are advantageous to design a low- power. The SDF FFT pipeline FFT is adopted. Complex constant multiplier is the architecture proposed and it includes a reconfigurable and bit parallel complex multipliers instead of using ROM's to twiddle factors storage.

In OFDM- MIMO systems, the information in the channel matrix is essential for decoding the message correctly transmitted. If the matrix channel is not accurately estimated, the channels cannot be fully decoupled at the receiver and the spatial streams coupled. For MIMO-OFDM estimator channel is FPGA implemented. The first requirement for reducing hardware resource is to select proper algorithm.

Channel estimator uses header-based Maximum method Likelihood (ML) special training symbols approach are transmitted before data packets are transmitted. Once received and detected the training in receiver symbols, the data received are preprocessed and modulated in domain frequency. Hence, frequency response of the channel is obtained in domain frequency, which is used for complexity computational reduction. Channel estimation block requires a number of operations and occupy many hardware resources and should be implemented efficiently with consideration of hardware area and performance. In the system block diagram section II of the OFDM - MIMO. Section III, presents FFT/IFFT architecture for application in wireless systems communication. In channel estimation section IV for MIMO-OFDM.

2. System Block Diagram

The architecture of the transmitter and receiver is illustrated in Fig. 2 and Fig.1 respectively. Scrambled bit stream and interleaved is separated into spatial streams by parser stream. Streams are mapped Secondly constellation into spatial. On the constellation thirdly, the points are through the STBC encoder to transform the spatial streams to time space streams.

Spatial mapper maps fourthly, space-time streams into chains transmit. Chains transmit are pilot inserted, modulated IFFT, CP (Cyclic Prefix), added then transmitted and modules RF. The signals transmitted are received through modules RF, DDC ADC, and CP remove. The chains received are modulated FFT, extraction pilot, and estimation channel and passed through the STBC decoder to transform to spatial streams from space-time stream. The spatial streams are inter leaved mapped, and the original bit stream is got by descrambled.

A. Scrambler

A scrambler is a device that manipulates a data stream transmitting before. Before an encoder a scrambler can be placed or it can be placed just before the modulation after the encoder. The manipulations are reversed by a descrambler at the side receiving. Accomplished scrambling by the addition of data to the original data or the changing of some important data of the original signal in order to make extraction of the original signal difficult.

B. Digital Up/Down Converter

The digital up converter (DUC) and the digital down converter (DDC) are important components of this system. The system is realized by carrier modulation/demodulation is by mixer and multiplier. The cascading technique is used for is implementing sample rate up/down through the Cascaded Integrator Comb filters(CIC), filter compensation and filter matched. CIC filter performs sample rate conversion by using only additions and subtractions not multipliers. But it has a droop shortcoming pass band, so we need a corresponding compensation filter to make the flat pass band. The make of the transmitter is by matched filter is used to and the receiver paired up and it can improve the SNR by reducing the noise.

C. Cyclic Prefix and Preamble

The cyclic prefix refers to the prefixing of data with an end of the repetition. As a guard interval, it eliminates the inter symbol interference from the data that occurred previously. The linear convolution is allowed by a selective frequency multipath channel to be modelled as circular convolution can be transformed by using FFT to domain in frequency. Synchronization is achieved by using Preamble and channel estimation at the receiver.

D. Space-Time Block Coding/Decoding

Alamouti's transmit diversity scheme with two transmit antennas and two receive antennas are used. A space-time block code is by using Alamouti's scheme is and suitable when two transmit antennas and an arbitrary number of receive are used in antennas. Characteristic of coding and decoding is the main and most important is made simple by Alamouti's scheme. A technique used is Space–time block coding is in wireless communications to transmit multiple copies of a data stream across a number of antennas and to exploit the various received versions of the data to improve the reliability of data-transfer.

E. Demapper

To reduce the complexity QAM demapper method is used of implementation and resources occupancy.

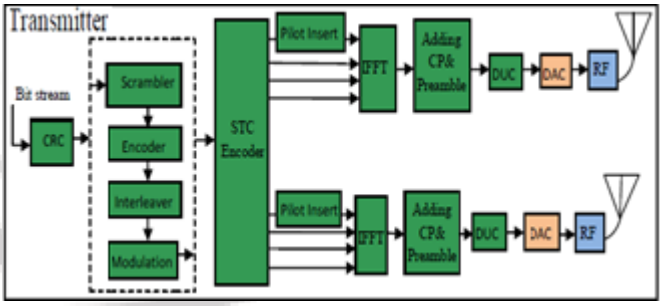


Figure 1: System Architecture of the Transmitter

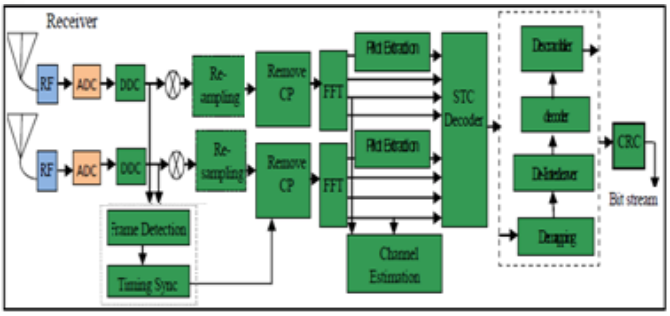


Figure 2: system architecture of the receiver

3. Proposed FFT/IFFT Architecture

A radix-2 64-point pipeline FFT/IFFT processor with low consumption of power, as shown in Fig.3. The architecture proposed is composed of three different types of processing (PEs) elements, delay-line (DL) buffers a complex constant multiplier, (as shown by a rectangle with a number inside), and some extra processing units by IFFT is computed. Here, the conjugate for extra processing units is easy to implement, the imaginary part which only takes the 2's complement of a complex value.

A barrel shifter can be substituted by using divided-by-64 module can be with In addition, for a complex multiplier constant in Fig.3, a novel reconfigurable complex constant multiplier is used to eliminate the twiddle-factor ROM. Proposed FFT/IFFT processor is the new multiplication structure has becomes the key component in reducing the chip area and power consumption.

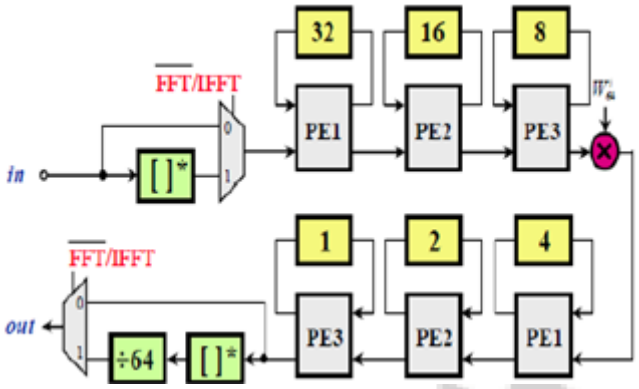


Figure 3: Radix–2 FFT 64 Point Pipeline FFT/IFFT

A. Processing Elements

Based on the radix-2 FFT algorithm, the three types of processing elements (PE3, PE2, and PE1) used in our design are illustrated in Fig. 4, Fig. 5, and Fig. 6, respectively. First

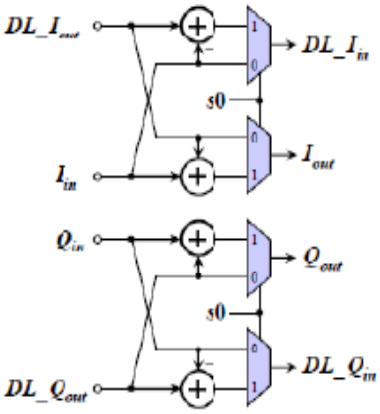


Figure 4: Circuit Diagram of PE3 Stage

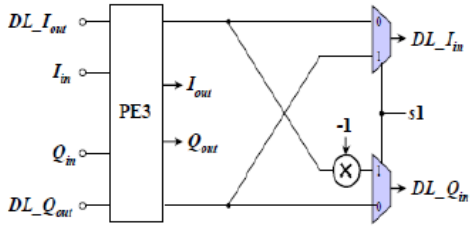


Figure 5: Circuit Diagram of PE2 Stage

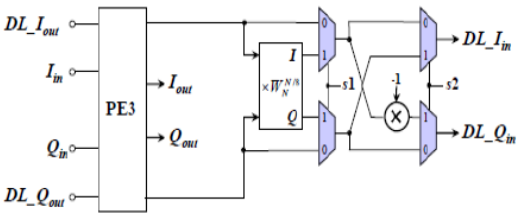


Figure 6: Circuit Diagram of PE1 Stage

the PE3 stage is used to implement a simple radix-2 butterfly structure only, and serves as the sub modules of the PE2 and Processing element PE1 stages. Iinare the real parts of the input data and andIout are the real parts of output data, respectively. Qin and Qoutdenote the image parts of the input and data output respectively. Similarly DL_Iinstand for the real parts of input and DL_Ioutstand for the real parts of output of the Delay buffers line, and DL_Qin are the inputs of imaginary parts and DL_Qoutare imaginary parts of outputs respectively.

B. Reconfigurable Complex Constant Multipliers

A reconfigurable low-complexity complex constant multiplier for computing is proposed. This structure of this complex multiplier also adopts a cascaded scheme to achieve low-cost hardware. Here, the meaning of two input signals (Iinand Iout) and two output signals (Qin and Qout) are the same as the signals in the PE1 stage.

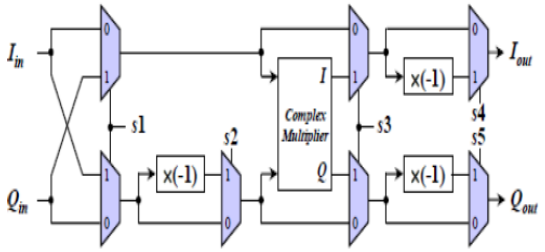


Figure 7: Reconfigurable Complex Constant Multiplier

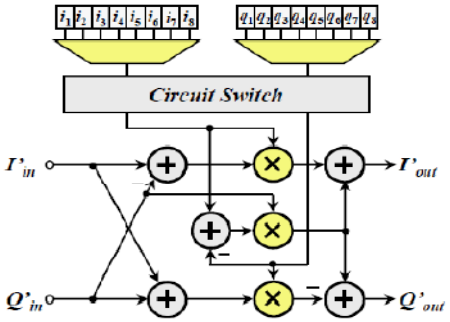


Figure 8: Complex Multiplier

this circuit is responsible for the computation of multiplication by twiddle factor in Fig.7, which is also an important circuit of FFT/IFFT processor. The word length multiplier used in Fig.8 adopts a low-error fixed-width booth multiplier for hardware cost reduction.

4. Channel Estimation for MIMO-OFDM

Header-based channel estimation with Maximum Likelihood algorithm is chosen to satisfy both the performance and less hardware resource utilization. Suppose X is a matrix of symbols being transmitted on a sub-carrier where the channel matrix is H. Hence, the channel estimation at receiver takes much less complicated operations after converting the received data to frequency domain. It makes hardware implementation simpler and hardware utilization smaller.

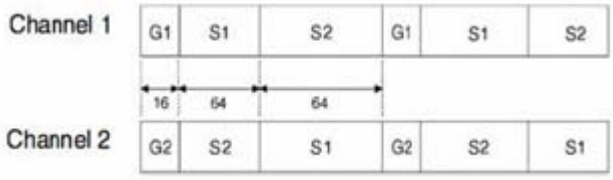


Figure 9: Structure of Training Symbols for Channel Estimation

Structure of channel estimation training symbols for 2 x 2 MIMO-OFDM is presented in Fig.9, where S1 and S2 indicate tone sequence 1 and tone sequence 2. Gl and G2 are the guard band of S1 and S2, respectively. Guard band is added for making cyclic extension of FFT symbols to avoid Inter Symbol Interference (ISI). S1, S2, G1, and G2 are repeated once again. Extra 3dB combining gain can be obtained by sending the same symbol two times. The number of arithmetic operation per the whole channel estimation symbols in Fig.9 is

(64 multiplications + 64 additions) × 4 (12)

Where 4 is the number of channels in 2 x 2 MIMO-OFDM. Finally, 160 MOPS can be obtained. This algorithm can be extended to support N x N MIMOOFDM in the same way as 2 x 2 MIMO-OFDM. That is, when X is unitary matrix in N-dimensions, Hij where i, j =0, 1, ... ,N can be obtained by using N sequences without decoding mixed channel. General concept to implement channel estimation algorithm on hardware is to deploy each processing logic and memory onto hardware domain as shown in Fig.10.

Each subcarrier delivers 1 bit signal adder and multiplier required should become simpler. ROM Txl and Tx2 store SI and S2sequence, respectively. Selects Switch block either ROM Txl or ROM Tx2 when either SI or S2 is received. RAM is needed to store intermediate channel coefficients which are calculated over maximum 4 frames. However, the baseline architecture still consists of O (n2) calculation blocks and memories in Figure 3. Instead, propose a pipelined architecture which uses only one block instead of O (n2) redundant blocks in Fig.11. 4μsec is taken for a pipeline stage period between RAM1 and RAM2 because a transmission period per one group of modulated data is 4 μ sec.

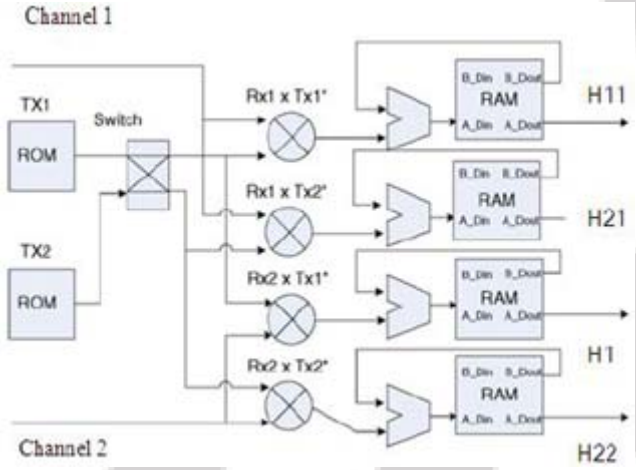


Figure 10: Architecture of Baseline Channel

Consider a 2 x 2 MIMO-OFDM system, in this RAM la and RAM 1b store data received by Rxl and Rx2, respectively. Each data carried by each sub-carrier is read from RAM 1 in serial. When system clock frequency is 20 MHz, 80 cycles are taken to process one frame. Only one group of 64 calculations is required to cover two receivers per each frame because each Rx data includes 32 valid data. To reduce processing time taken by the calculation block, higher sampling frequency is used during channel estimation stage between RAM 1 and RAM 2 in Fig.11.

Dual-port RAM is deployed to reduce latency and support different data access. Input data stored in RAM la and RAM 1b are read every even clock and odd clock, respectively. Then, those data are processed through the calculation block, and stored into RAM 2 at 100 MHz while RAM 2 transfers estimated channels at 20 MHz 100 MHz is enough to support 64 calculations within 4 μ sec. In Fig.11, the calculation block includes only adders and RAMs without multiplier. Multiplier and ROM are not necessary because training symbols are 0 or ±1.

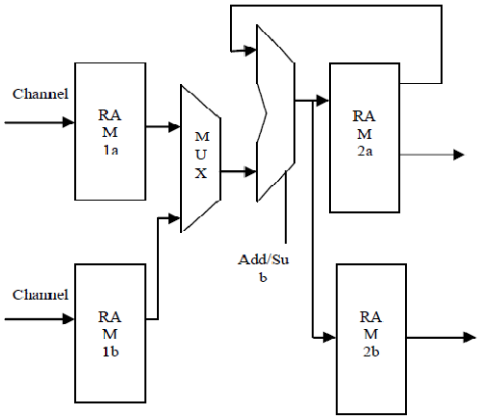


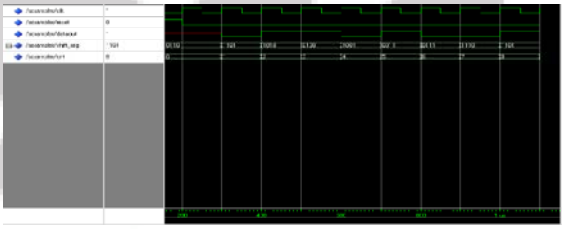
Figure 11: Architecture of New Channel Estimator

Adders can be used as subtractors. The calculation block is so simple that additional pipeline buffers are not needed. It means that critical path delay in channel estimator should be much shorter than system clock period. If two repeated sequences are used to improve performance, total 2 frames are taken to obtain channel estimation result. 3 x 3

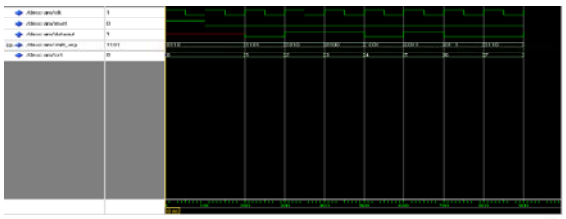
MIMO-OFDM can be extended from 2 x 2 MIMOOFDM in the same way. Only one group of 64 calculations is required to cover three receivers per each frame because each Rx data includes 21 or 22 valid data. Architecture in Fig.11 is also the same except the number of pipeline RAMs. Estimated channel coefficients can be obtained after processing data over 3 frames. New channel estimator architecture also supports more channels in MIMO-OFDM system.

5. Simulation Results

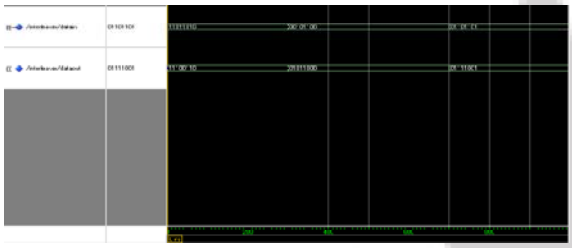
A. Simulation Result of Scrambler



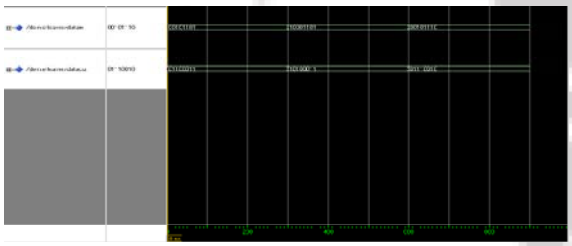
B. Simulation Result of Descrambler



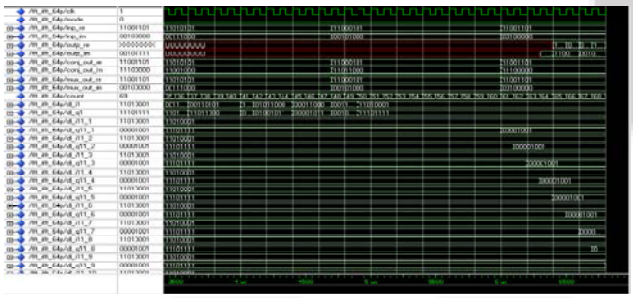
C. Simulation Result of Interleaver



D. Simulation Result of Deinterleaver



E. Simulation Result of Pipeline FFT/IFFT Processor



6. Conclusion

A flexible MIMO-OFDM system is presented in this paper. Some necessary receiver and transmitter algorithms, such as channel estimation, OFDM synchronization, encoding and decoding of STBC, modulation, demapper, scrambler, descrambler, interleaver, de-interleaver and other components are implemented in FPGA.

A novel ROM-less and low-power pipeline 64-point FFT/IFFT processor for MIMO-OFDM applications have been described to lower hardware cost and power consumption compared to other architectures. An efficient channel estimation block for 2 x 2 MIMO-OFDM implementation results in terms of resource utilization as well as performance. More channels can be supported by using our proposed architecture. The future scope of this project is to add the noise in the system and the estimation of channel using different channel models is to be carried. Channel estimation and compensation for different channel models for delays also to be implemented.

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Author Profile

M. Arun Kumar received the Bachelor of Engineering degree in Electronics and Communication Engineering from Maharaja Institute of Technology Arasur Coimbatore, India, in 2010 and received Master of Engineering degree from the Department of VLSI Design, from Sri Ramakrishna Engineering College, Coimbatore, India, in 2013. He is currently working as Assistant Professor at Karpagam College of Engineering, Coimbatore. His area of interest includes Digital Signal Processing, Low power VLSI Design.