

Speed Analysis of Body Biased TSPC and ETSCPC Flip Flops

Nemitha B¹, Pradeep Kumar B. P²

PG Student, Dept. of ECE Akshaya institute of technology, Tumkur, Karnataka, India¹
Assistant professor, Dept. of ECE, Akshaya institute of technology, Tumkur, Karnataka, India²

Abstract: In this paper the Performance of body biased True Single Phase Clock (BBTSPC) and body biased Extended True Single Phase Clock (BBETSPC) are investigated. The delay of BBTSPC and BBETSPC are analyzed, simulated and compared with the existing TSPC and ETSPC. A high speed divide-by-2/3 unit of prescaler with the body biased is proposed and validated that this prescaler can operate with higher frequency of 4 GHz stably on a 180 nm technology. This prescaler with the body bias design can be widely used in Communication data analysis probe systems.

Keywords: CMOS integrated circuit, D flip-flop (DFF), frequency divider, frequency synthesizer, high-speed digital circuit, phase-locked loops (PLLs), true single-phase clock (TSPC)

1. Introduction

Dual modulus prescaler is important circuit block used in frequency synthesizers. To divide the high frequency signal from the voltage controlled oscillator (VCO) to a low-frequency signal by a predetermined divide ratio, either (N+1) or N, which is controlled by a swallow counter. The prescaler is a synchronous circuit which is formed by D flip-flops and additional logic gates. Due to the incorporation of additional logic gates between the flip-flops to achieve the two different division ratios, the speed of the prescaler is affected and the switching power increases. Various flip-flops have been proposed to improve the operating speed of dual-modulus prescalers. The optimization of the D flip-flop in the synchronous stage is essential to increase the operating frequency and reduce the power consumption. The high speed operation of MOS transistors is limited by their low transconductance. Therefore, dynamic and sequential circuit techniques or clocked logic gates such as, true single phase clock must be used in designing synchronous circuits to reduce circuit complexity, increase operating speed, and reduce power dissipation.

Figure 1.1 shows a generic PLL (phase locked loop) based synthesizer. The reference divider R can be used to scale highly accurate crystal based input frequencies down to desired levels for the PLL module. The PLL consists of a phase-frequency detector (PFD) and a loop filter (LF) apart from the VCO. The operation of the PLL and the programmable counter in the feedback path allow generation of accurate high frequencies from a pure low frequency signal. The programmable P-counter is usually preceded by a prescaler ($\div N$) that scales down the high output frequencies to a range at which standard CMOS dividers can be implemented.

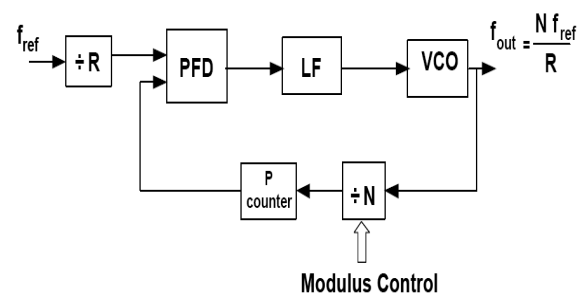


Figure 1.1: A typical integer-N PLL frequency synthesizer

A dual-modulus division gives the flexibility to select channels on the basis of the number of times each of the module is selected. The dual-modulus prescaler could also be used in the feedback to obtain fractional output frequencies. Such synthesizer architectures, called fractional-N frequency synthesizers, allow the reference frequencies to be higher. PLL stability considerations require loop bandwidths to be a fraction of the reference frequency. So fractional-N synthesizers allow for higher loop bandwidths, resulting in faster output settling and lower oscillator noise characteristics. The power consumption and frequency of operation of TSPC and E-TSPC 2/3 prescalers are to be analyzed and an ultra-low power TSPC 2/3 prescaler is designed. Based on this design a 32/33 prescaler is then implemented, which is highly suitable for high resolution fully programmable frequency synthesizers.

2. Related Research

In this paper the power consumption and operating frequency of true single phase clock (TSPC) and extended true single phase clock (E-TSPC) frequency prescalers are investigated. Based on this study a new low power and improved speed TSPC 2/3 prescaler is proposed which is silicon verified. Compared with the existing TSPC architectures the proposed 2/3 prescaler is capable of operating up to 5 GHz and ideally, a 67% reduction of power consumption is achieved when compared under the same technology at supply voltage of 1.8 V This extremely low power Consumption is achieved by radically decreasing the sizes of transistors, reducing the number of switching

stages and blocking the power supply to one of the D flip-flops (DFF) during Divide-by-2 operation [1].

In this paper the short-circuit power and the switching power in the E-TSPC-based divider are calculated and simulated. A low-power divide-by-2/3 unit of a prescaler is proposed and implemented using a CMOS technology. Compared with the existing design, a 25% reduction of power consumption is achieved [2]. In this paper the E-TSPC logic based divide-by-2/3 prescaler suitable for low supply voltage (0.9V) and low power applications is designed and implemented wherein the counting logic and the mode selection control are implemented using a single transistor. Thus the critical path is reduced which in turn enhances its working frequency. Compared with the conventional TSPC and E-TSPC based 2/3 prescaler designs as much as 46% in PDP, 24% in operation speed and 44% in area can be achieved by the proposed design. Also a 32/33 prescaler, 47/48 prescaler and a multi modulus 32/33/47/48 prescaler which incorporates the proposed 2/3 prescaler are designed and implemented [3].

In this paper True Single Phase Clock (TSPC) based on Ratio logic D flip-flop and Transmission Gates (TGs) is implemented in 0.18 μ m CMOS process. A Glitch elimination TSPC D-flip flop is used in the synchronous counter. TGs are used in the critical path and the control logic for mode selection. The power efficient TSPC design technique is applied to 3/4 and 15/16 prescalers, and their performances are compared. Simulation and measurement results show high-speed, low-power, low PDP and multiple division ratio capabilities of the power efficient technique with a frequency range of 0.5-3.125GHz. The improved speed, the power efficiency, and the flexibility will promote its wide deployment in Multi gigahertz range applications [4].

3. Methodology

As shown in Fig.3.1. (a) And (b) an E-TSPC flip-flop uses only two transistors while a TSPC flip-flop uses three transistors. Of various dynamic logic CMOS circuit techniques, TSPC dynamic CMOS circuit is operated with one clock signal only to avoid clock skew problems. A True Single Phase Clock (TSPC) flip-flop configured to operate in an evaluating and an hold (pre-charge) mode, comprising as integral parts: an input stage having an input node and a first output node, a middle stage having a second output node, an output stage having a third output node, and a reset functional block being switchable between an activated and an deactivated mode. The reset functional block resets the flip-flop when activated and is configured to synchronous exit out of reset when switched from its activated to its deactivated mode so that an output signal of the flip-flop is only up-dated when the flip-flop changes to its next evaluating mode. TSPC flip-flops are clocked by a clock signal which alternates between a first state associated with the evaluating mode and a second state associated with the hold mode. Substantially, the output signal of an embodiment of the inventive flip-flop is present at the third node; if necessary, the signal at the third node may be inverted by an inverter. The output signal of the embodiment of the inventive flip-flop can have two states, namely logical

value "1", usually associated with a high voltage and logical "0", usually associated with a low voltage. When the embodiment of the inventive flip-flop is reset, then the output signal is set to logical "0". Since the reset function is a synchronous exit out of reset function, the output value of the flip-flop must only be up-dated with the edge of the clock signal changes from its hold mode to its evaluating mode when the reset is deactivate.

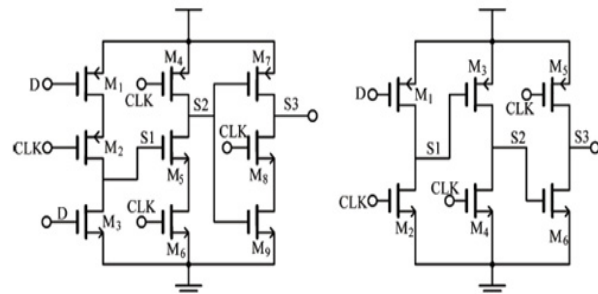


Figure 3.1 (a): TSPC flip-flop. (b) E-TSPC flip-flop

In the proposed method the body pin of the transistor is connected to source and applied some positive voltage with respect to source. In this body biasing technique the drain current is decrease and threshold voltage is increase this is due to body effect of MOS transistor. Hence the total power consumption is decrease.

4. Simulation and Results

The simulations are performed for all the above mentioned State-of-art TSPC and E-TSPC using the Mentor Graphics Software and the Chartered 0.18 um CMOS technology.

4.1 Body biased TSPC

Figure.4.1 (a) shows the schematic diagram of body biased TSPC, which was simulated in Mentor graphics software. Figure.4.1 (b) shows the waveform of body biased TSPC. In this waveform shown there is the switching in the output for every raising edge of the clock. And this makes the perfect operation of the D Flip flop in TSPC logic.

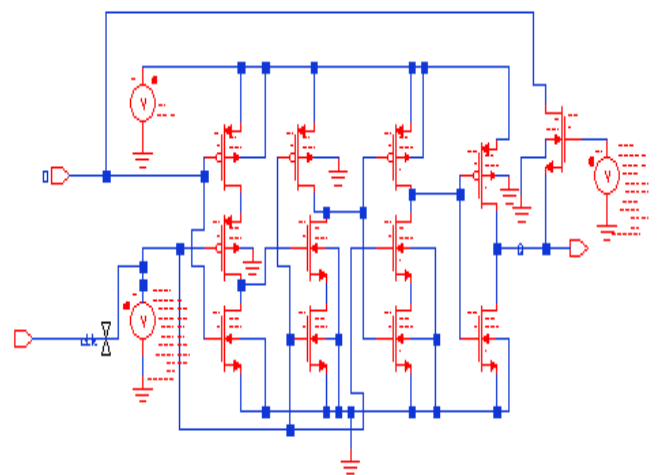


Figure 4.1(a): Schematic diagram of body biased TSPC

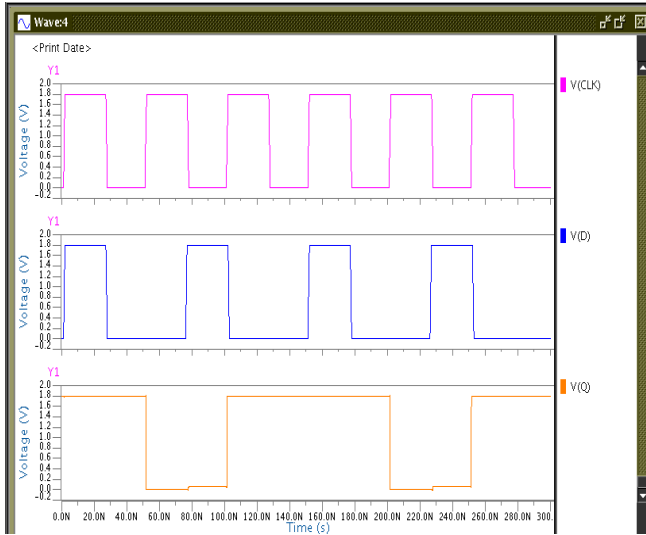


Figure 4.1 (b): Waveform of body biased TSPC

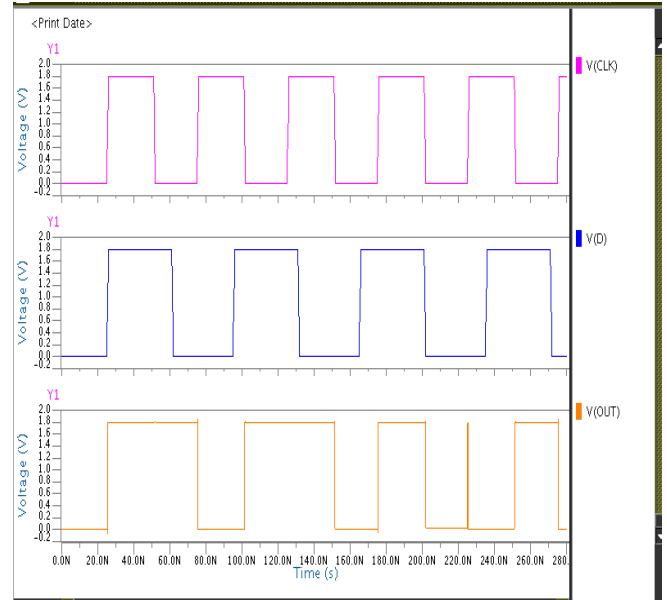


Figure 4.2 (b): Waveform of body biased E-TSPC

4.2 Body biased ETSPC

Figure 4.2 (a) shows the schematic diagram of body biased ETSPC, which was simulated in Mentor graphics software. Figure.4.2 (b) shows the waveform of body biased ETSPC Output is divide by two of clock frequency.

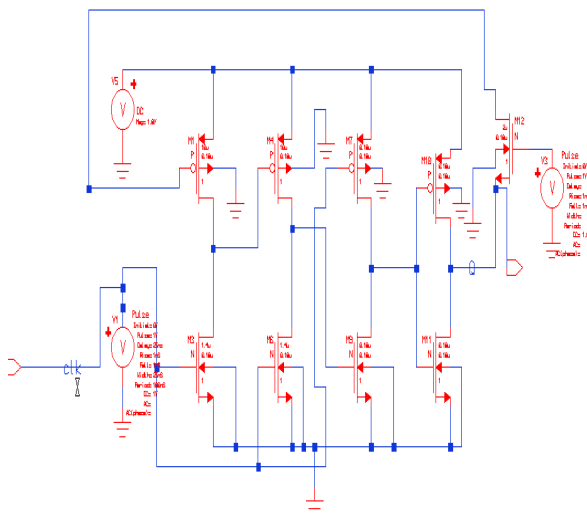


Figure 4.2 (a): Schematic diagram of body biased E-TSPC

Figure 4.3 show the delay comparison of TSPC, ETSPC, and body biased TSPC, body biased ETSPC. Delay of simple TSPC is 2 ns and ETSPC is 1 ns, whereas Delay of body biased TSPC is 0.6 ns and body biased ETSPC is 0.2 ns. So, Body biased logic is faster. This is because of body biased threshold voltage decreases, so delay decreases.

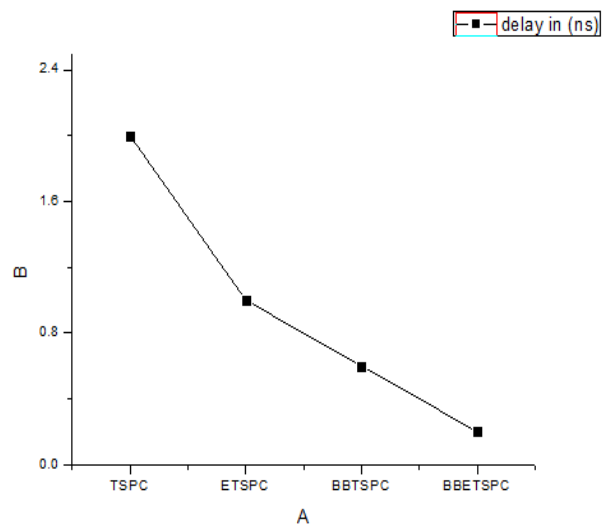


Figure 4.3: delay plot of simple and body biased TSPC and ETSPC

5. Conclusion

From above analysis, it is observed that the TSPC and ETSPC flip-flop has more delay. In case of body biasing circuit, the delay is low compare to other logic discussed here because of decrease in threshold voltage. It has less delay and power delay product than the simple true single phase clock (TSPC) and extended true single phase clock (ETSPC) flip flop. Therefore body biasing extended true single phase clock (BBETSPC) flip flop has better performance compare to other flip flop.

References

- [1] Yeo, Kiat Seng Boon, Chirn Chye Lim, Wei Meng, Do, Manh Anh, Krishna, Manthena Vamshi." Design and analysis of ultra low power true single phase clock CMOS 2/3 prescaler." IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 57, NO. 1, JANUARY 2010.
- [2] Yu, Xiao Peng, Do, Manh Anh, Lim, Wei Meng, Yeo, Kiat Seng, Ma, Jianguo." Design and optimization of the extended true single phase clock-based prescaler." IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, VOL. 54, NO. 11, NOVEMBER 2006.
- [3] Anish M George, Prof. Riboy Cheriyann" Design and Analysis of Power and Area Efficient 2/3 Prescaler Using E-TSPC Logic "International Journal Of Scientific & Engineering Research, Volume 4, Issue 8, August 2013 ISSN 2229-5518.
- [4] Ramesh.K, E.Velmurugan, G.Sadiq Basha." Design of Low Power Cmos High Performance True Single Phase Clock Dual Modulus Prescaler". Int. Journal of Engineering Research and Applications ISSN: 2248-9622, Vol. 3, Issue 5, Sep-Oct 2013.
- [5] YUAN JI-REN, INGEMAR KARLSSON, AND CHRISTER SVENSSON "A True Single-Phase-Clock Dynamic CMOS Circuit Technique" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-22, NO. 5, OCTOBER 1987.
- [6] J. Navarro Soares, Jr., and W. A. M. Van Noije "A 1.6-GHz Dual Modulus Prescaler Using the Extended True-Single-Phase-Clock CMOS Circuit Technique (E-TSPC)" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 34, NO. 1, JANUARY 1999.
- [7] Fernando P. H. de Miranda, Joho Navarro SJr., Wilhelmus A.M. Van Noije "A 4 GHz Dual Modulus Divider-by 32/33 Prescaler in 0.35µm CMOS Technology" July 10, 2010 from IEEE Xplore.
- [8] Jiren Yuan and Christer Svensson "New single-clock CMOS latches and flipflops with improved speed and power savings" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 32 NO. 1, JANUARY 1997.
- [9] H. Oguey and E. Vittoz, "CODYMOS frequency dividers achieve low power consumption and high frequency," Electron. Lett., pp. 386–387, Aug. 1973.
- [10] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits, A Design Perspective, ser. Electron and VLSI, 2nd ed. Upper Saddle River, NJ: Prentice-Hall, 2003.
- [11] C. Lam and B. Razavi, "A 2.6-GHz/5.2-GHz frequency synthesizer in 0.4-µm CMOS technology," IEEE J. Solid-state Circuits, vol. 35, no. 5, May 2000.



Mr. Pradeep Kumar .B .P, He is presently working as a Assistant Professor in Akshaya Institute of Technology, Tumkur and perusing his PhD in Jain university in electronics & Communication engineering department. He has published more than 29 technical papers in national and International Journals and conferences. His areas of interests are signal processing, Medical Imaging, pattern recognition, video processing, Multimedia Communication systems.

Author Profiles



Ms. Nemitha B received the BE degree from Geetha Shishu Shikshana Sangha Institute of engineering and Technology for women, Mysore. She is presently pursuing PG in Akshaya Institute of Technology, Tumkur. She has presented 6 technical papers in national conferences. Her areas of interests are VLSI, speech processing, Medical electronics, Multimedia Communication systems.