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Low Power Circuit Design Using Positive Feedback Adiabatic Logic (PFAL)

Arjun Mishra[1], Neha Singh[2]

[1]Amity University, Department of Electronics and Communication Engineering, ASET, Noida, Uttar Pradesh, India

[2]Banasthali Vidyapith, Department of Electronics, Banasthali, Tonk, Rajasthan, India

Abstract: ***This paper presents an adiabatic logic family called positive feedback adiabatic logic circuits (PFAL).There is power reduction due to energy recovery in the recovery phase of the clock supply. The power dissipation comparison with the static CMOS logic is performed. The simulation is performed on cadence virtusuo using 180nm CMOS technology. The result shows that power reduction of 50% to 70% can be achieved over static CMOS within a practical operating frequency range.***

Keywords: Adiabatic, CMOS, PFAL, ECRL, N-MOS, P-MOS.

1. Introduction

An adiabatic switching is an approach to reduce power dissipation in the digital logic at cost of slower speed of operation. It allows the energy store on the circuit capacitance to get recycled instead of dissipated as heat [1].It is also knows as reversible logic circuit. In conventional CMOS switch, the switching power dissipation has lower limit of $C_L Vdd^2/2$, cannot be reduced lower then this limit. For energy recovery circuit in adiabatic switching the energy dissipation when a capacitor C charge from 0 to V_{dd} or discharged from V_{dd} through the resistance R during time T is given as

$$E=\left(\frac{RC}{T}\right)CV_{dd}^2$$

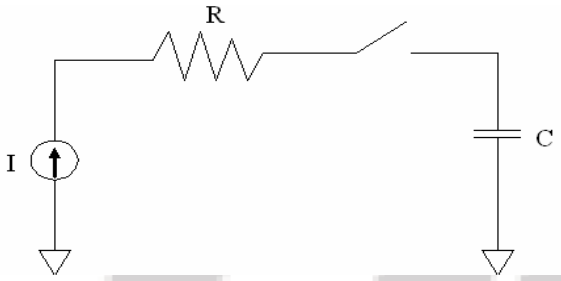

Figure 1: Circuit representing adiabatic switching

Where R is resistance of the P-MOS network and C is load capacitance.

When T>>RC, the power consumption is much lower than the conventional CMOS circuit for which energy dissipation is $(CV_{dd}^2/2)$ during charging and discharging.

There are various adiabatic logic technique [2]-[4] are available among them partially adiabatic technique is efficient in term of number of device and silicon area.

This paper describe a one of the partial adiabatic technique called as positive feedback adiabatic logic circuit (PFAL) with cross coupled devices (N-MOS,P-MOS) connecting two nodes that form the true and complementary output. It gives best performance in terms of energy consumption, useful frequency range, and robustness against technology variation. The basic PFAL logic design and operation will be presented. The energy dissipation comparison of PFAL adiabatic logic and static CMOS logic is made. The 2:1 multiplexer and 1-bit full adder is made using PFAL to evaluate performance in cadence virtuoso tool.

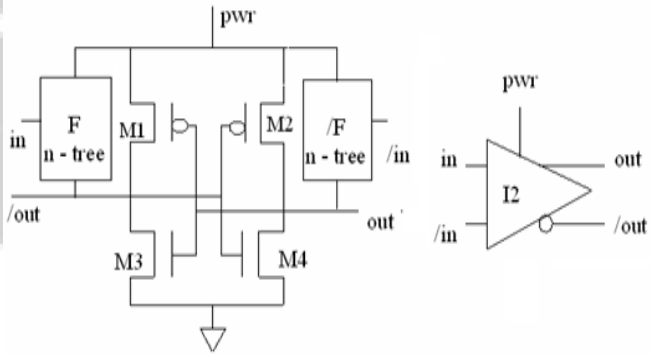

Figure 2 (a)

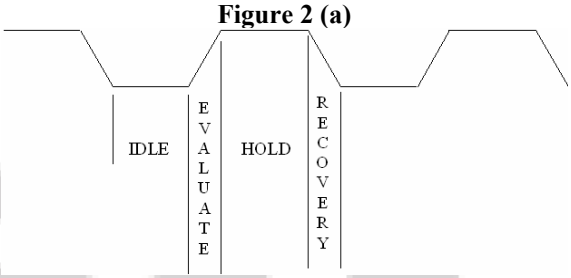

Figure 2 (b)

Figure 2: (a) General PFAL schematic (b) Four –phase pulsed power supply

2. Logic Design and Operation

The partial energy recovery structure PFAL [5] offers lowest energy consumption compare to other families and a good robustness against technology parameter variations. The general schematic of PFAL is shown in fig 1 (a).It is dual – rail circuit with partial energy recovery. The core of all PFAL gates is an adiabatic amplifier, a latch made by two PMOS M1-M2 and two NMOS M3-M4 that avoids logic level degradation at output nodes out and /out. The two n-tress realize the logic function and gives complimentary output. The functional block is in parallel to PMOSFETs of adiabatic amplifier and form transmission gates that offers

low equivalent resistance when need to charge the capacitance.

PFAL uses four phase Let us assume in is at high and /in is at low. At beginning of cycle, when power clock rise from 0 to $V_{dd,}$ out remains at ground level and /out flows power through F (n-tree).When power clock reaches at V_{dd} the output hold the valid logic. These values are maintained during hold phase and use as input to next stage. After hold stage power clock down to 0 so that /out return its energy to power clock so that deliver charge is recovered.

3. Simulation Results

To compare the power dissipation with static CMOS and PFAL adiabatic logic the circuit simulation is performed using Cadence Virtuoso. The technology used for simulation is 180 nm CMOS technology with 3v power supply. The input data rate for CMOS is made identical to that of adiabatic circuit. The comparison requires developing the circuit schematic based on both static CMOS and PFAL technique. Each circuit is simulated for different frequency and corresponding dynamic power is calculated through the tool. Figure 2(a) and Figure 2(b) shows the 2:1 mux PFAL schematic and the full adder PFAL schematic respectively. Figure 3 shows the power versus frequency response for static CMOS and PFAL adiabatic circuit.

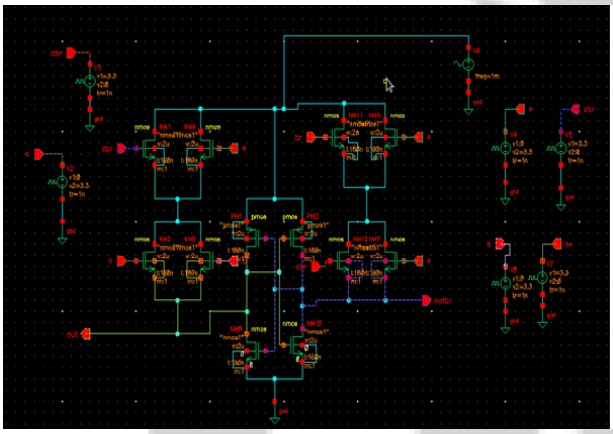

Figure 2 (a): 2:1 Mux schematic PFAL

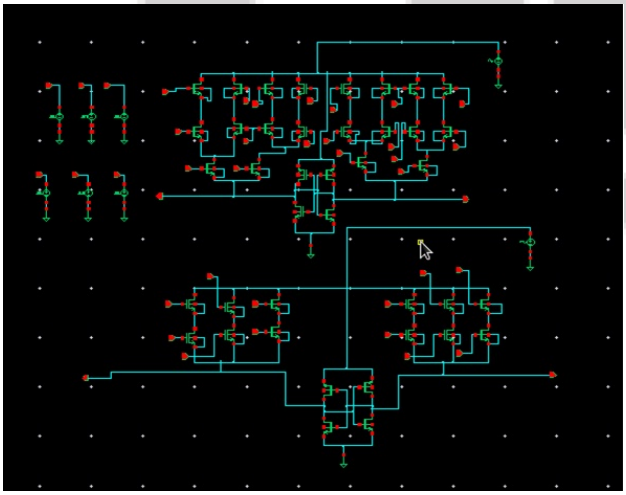

Figure 2 (b): Full Adder PFAL

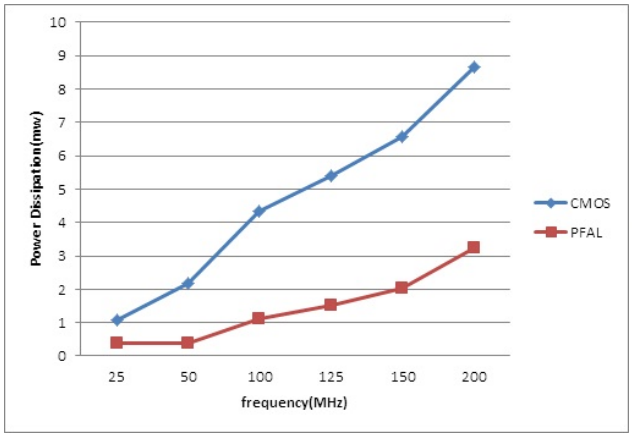

Figure 3 (a): Power versus Frequency for 2:1 Mux

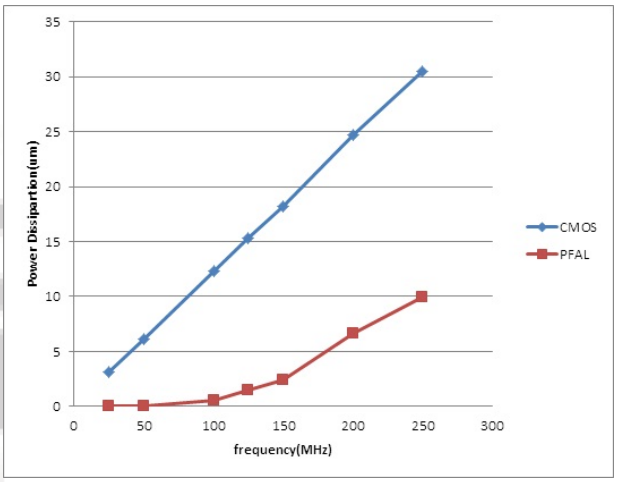

Figure 3 (b): Power versus Frequency for Full Adder

From figure 3 (a) and 3 (b) shows that for given power supply and frequency the PFAL circuits have better power performance compared to static CMOS. The power consumption in static CMOS increases linearly with clock frequency for static CMOS since the dynamic power dissipation in static CMOS is directly proportional to clock frequency [6].

4. Conclusion

The adiabatic PFAL offers significant power reduction and so better power performance over conventional static CMOS. The comprehensive simulation shows that PFAL circuit can recover 50% of the energy dissipated in conventional static CMOS logic. However the PFAL suffers from large switching time, so it is not suitable to application where the delay is critical. Thus suffer from low speed of operation and is not suitable for the application where fast switching is required.

5. Acknowledgment

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Author Profile

Arjun Mishra, received the B.Tech degree in Electronics and Communication Engineering from Dr R.M.L Avadh University, Faizabad, India, in 2011.He is currently final year student of M.Tech in VLSI from Amity University, Noida. His research interest includes low power circuit designing, digital design, fundamental study of IC fabrication and fabrication of micro- or nanostructured surfaces.

Neha Singh received the M.Tech degree in VLSI from Banasthali Vidyapith, Banasthali, Tonk, Rajasthan, India, in 2013.She has attended and published some papers in national conference. She is currently working as Design Engineer at Infosys. Her research interest includes MEMS, IC fabrication, analog and digital designing, thin film transistor and layout designing**.**