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A 2.4 GHz Reference-Less Receiver for QPSK Demodulation

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Abstract: ***In this paper we will design a novel idea for a single chip wireless QPSK receiver without resort to extra resonator based reference. In contrast to conventional architectures, the receiver recovers the RF carrier frequency directly from the incident radio signal for frequency down conversion. Meanwhile, the model designed will accomplish frequency acquisition and also phase and frequency tracking as well as QPSK demodulation simultaneously. This design is a 2.4GHz reference-less single chip wireless receiver for QPSK demodulation .The designed receiver will accomplish Local Oscillator carrier recovery and data demodulation directly from the RF received signal without resort to resonator based reference, such as crystal oscillator but by using the designed Carrier recovery loop.***

Keywords: Carrier recovery, QPSK, reference-less, wireless receiver, demodulation.

1. Introduction

In recent years Wireless sensor network and bio-inspired electronics have drawn tremendous research efforts recently. For the sensor node integrated circuits design, small form factor, low power, and system cost are of special interests to promote pervasive and ubiquitous adaptations. Conventionally, RF receiver front-end includes a LO (local oscillator) generator that utilizes crystal or other resonator based reference for carrier frequency synthesis. The crystal oscillator itself in general dissipates extra power and is too bulky for single chip integration. Meanwhile, due to unavoidable crystal frequency mismatches between the transmitter and receiver side, timing recovery loop is required at the digital base band compensate frequency offset for data demodulation. These issues motivate this research work of developing a single chip wireless receiver which recovers the LO frequency directly from the received RF signal. Based on the concept of wireless remote frequency synchronization to the transmitter side, it eliminates extra reference generator at the receiver side and also facilitates wireless clock distribution. Since the LO carrier at the receiver side is tracking the frequency at the transmitter side directly during data receiving, frequency offset problem between the transmitter and receiver in conventional wireless transceivers is eliminated. Meanwhile, it accomplishes data demodulation along with carrier and timing recovery without resort to extra base-band ADC .

2. Architecture Implementation

An experimental prototype for QPSK wireless receiver at 2.4 GHz is implemented to demonstrate this concept. Figure.1 shows the proposed architecture. It integrates LNA, mixer channel selection filter, post amplifier, data demodulator, frequency discriminator, and LO carrier recovery loop (CRL) on a single chip. The LNA is based on differential gain boosted common gate architecture to compromise between power consumption and broad band input matching. Double-balanced Gilbert mixer with current injection is employed to lower the noise contribution from commutating stage while sustain the conversion gain. As a single channel experimental prototype, the interference is rejected by both external band selection filter and on chip channel selection filter. The LNA and mixer help in down conversion and noise reduction respectively. The CRL composes of a VCO, prescaler, divider and multiphase generator, phase selector (MUX), and a gating phase frequency detector (GPFD). Incorporating with the data demodulator, it recovers carrier frequency and clock from the QPSK modulation signal for frequency down conversion and data demodulation.

A. Frequency Acquisition

Let the cascade divide ratio of the prescaler and feedback divider be N, f_{LO} denote the VCO frequency, and f_{IF} represent the IF frequency. At the onset for data receiving, a constant phase preamble (f_{RF}) from the transmitter is received, and the voltage controlled oscillator (VCO) is preset to its highest frequency which is larger than f_{RF}. During this mode, the CRL is operated in the frequency acquisition mode. Meanwhile, the phase selector (MUX) passes a fixed divider output phase (one of φ0,.., φ7) to the GPFD. The down converted signal f_{IF}, where $f_{IF} = f_{LO} - f_{RF}$ is then compared to f_{LO}/N by the GPFD. If $f_{LO} - f_{RF} > f_{LO}/N$, f_{LO} decreases so that f_{IF} is reduced more than f_{LO}/N for $N > 1$. Contrarily, if $f_{LO}/N > f_{LO} - f_{RF}$, f_{LO} increases so that f_{IF} is increased more than f_{LO}/N. By the negative feedback mechanism, when the loop is settled. As illustrated in 1(b). The frequency locking detector is realized by a frequency discriminator Figure. 2 illustrates detailed circuit schematic, which is based on the concept of edge counting .As is described in (1), when the loop approaches locked, the IF frequency would be equal to the divider output In order to improve the resolution for frequency detection, is scaled down by to generate a control signal . The high and low level of alternatively performs as gating pulse of, whose counting edges are stored in two latches. In this design, if the contents of latches fall within , the confident counter will be toggled. When the contents in latches hit the target consecutively, implying that approaches locked state, and the status of frequency locked is then resolved by the confident counter.

B. Phase Tracking and Data Demodulation

When the loop approaches locked, the receiver will acknowledge transmitter for data receiving. The mode control signal (Mod_CTL) will then switch the CRL to phase tracking mode, as illustrated in Figure. 1(c). Afterwards, the CRL will keep track the carrier frequency as well as demodulate the QPSK signal simultaneously. Figure. 3 illustrates the scheme for QPSK demodulator and timing diagram for the gating PFD. At the post amplifier output, the fIF switches its phase among (0, 90, 180, and 270 degrees) periodically at symbol rate (fs), as is shown in Figure. 3(a). For QPSK demodulation, the divider output fd (fd = fLO /N) generates 8 phases (φ0, ., φ7) to capture fIF. Here (φ0, φ2, φ4, φ6) divides the signal constellation into 4 zones, and the IF signal is directly demodulated by detecting the operating zones (I, II, III, IV) that fIF falls into. This is accomplished by sampling (φ0,..,φ7) using fIF followed by edge detector and decoder. The I/Q digital output is then demodulated after confident counter, as shown in Figure 3(b). In each phase zone, the targeted phase for frequency tracking and phase synchronization is (φ1, φ3, φ5, φ7) respectively. The demodulator then switches its corresponding targeted phase according to the demodulated I/Q data through the MUX to the GPFD. Thus the CRL can continuously track the RF signal . To avoid misdisturbing the carrier frequency during phase switching in QPSK signaling, a timing controller in the demodulator will generate gating pulse (GP) to enable the GPFD, as also shown in Figure.3 (c).

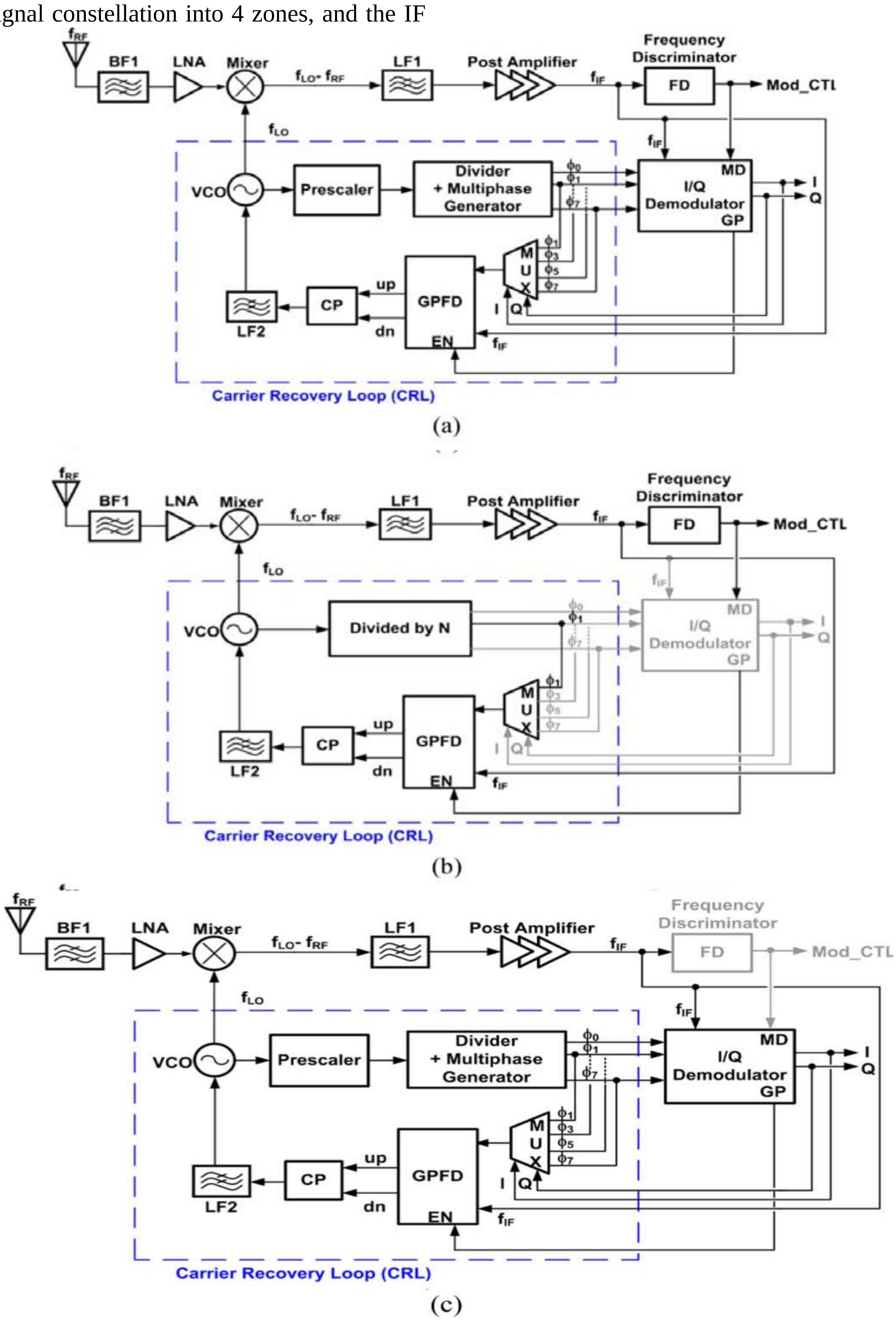


Figure 1: (a) Proposed receiver architecture. (b) Frequency acquisition mode. (c) Phase tracking and data demodulation mode.

3. Building Blocks

A. Low Noise Amplifier

Conventionally, low noise amplifiers in RF receiver are based on common-source or common-gate architectures, as are shown in Figure. 4. A common-source LNA (CSLNA) in general has better noise performance compared to its common-gate counterpart (CGLNA). However, it requires two on-chip inductors for narrow band input matching contrarily; CGLNA only needs a single inductor for input matching. Gain boosting can provide broadband matching depending on the quality factor of the resonator .By using the designed LNA It can reduce the power consumption as well as noise in the circuit so a gain boosted technique is used with CGLNA.

B. Carrier recovery loop

The carrier recovery loop consists of a VCO, prescaler, divider, multiphase generator, phase selector (MUX), and a gating phase frequency detector (GPFD). Incorporating with the data demodulator, it recovers carrier frequency and clock from the QPSK modulation signal for frequency down conversion and data demodulation.

To alleviate reference spurs charge pump and loop filter is employed. The divider chain in the feedback path of the CRL is composed of a high speed divided-by-19 divider followed by a divided-by-8 divider, as shown in Figure5. The divided-by-19 divider is composed of a 4/5 prescaler, a divide-by-4 divider and a control logic. Figure 5(b) shows the timing diagram. To reduce power dissipation as well as propagation delay, TSPC flip-flops with embedded NAND gates are incorporated in the dividers, as shown in Figure.5(c). The synchronous divided-by-8 divider also performs as a multiphase generator. Figure 5(a) shows the circuit schematic. The 8 phases output signals are then utilized to capture QPSK symbols, and one of them is passed to the GPFD for phase tracking.

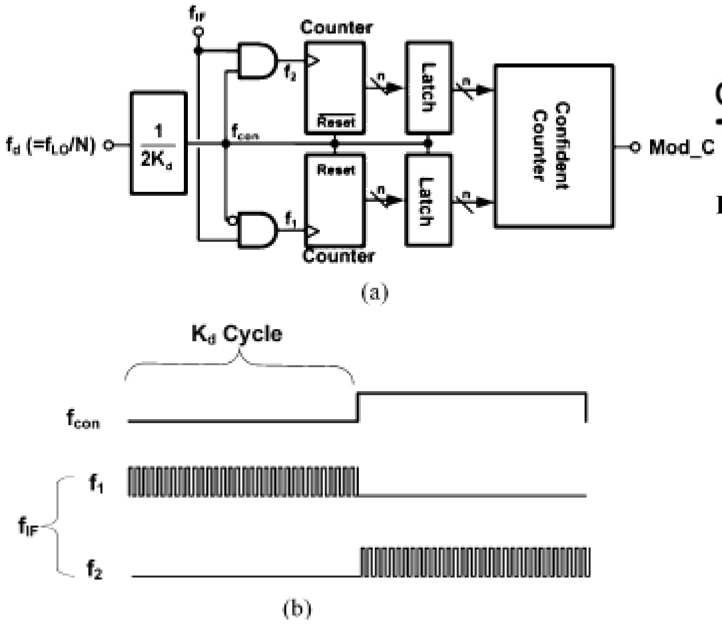


Figure 2: Frequency discrimination and edge countering.

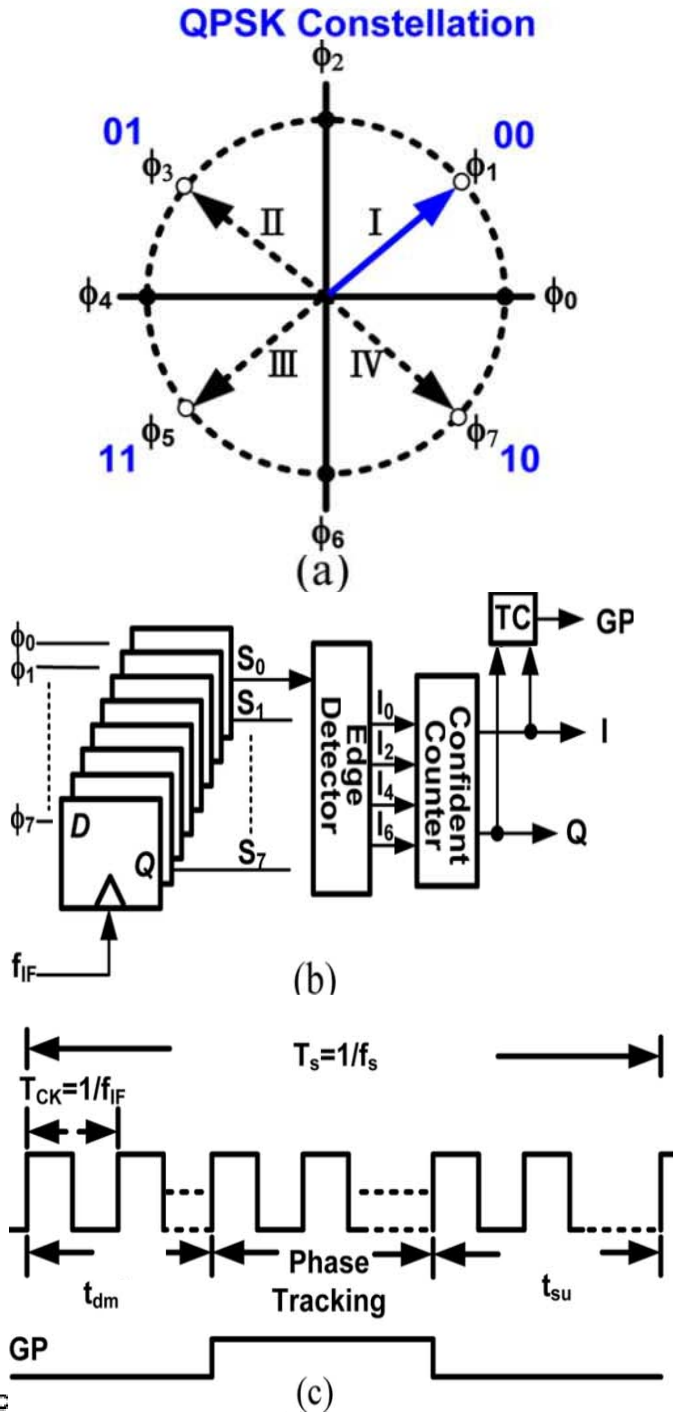


Figure 3: (a) QPSK signal constellation. (b) Demodulator. (c) Timing diagram

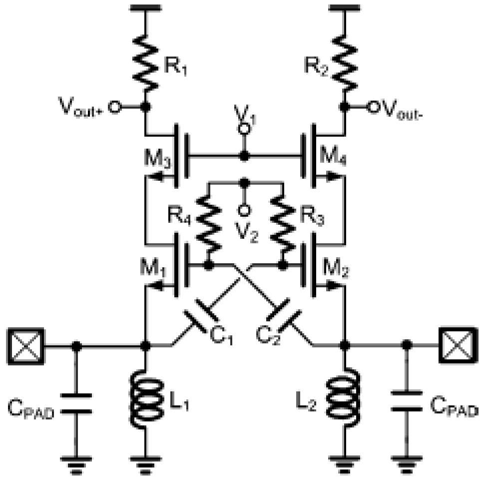
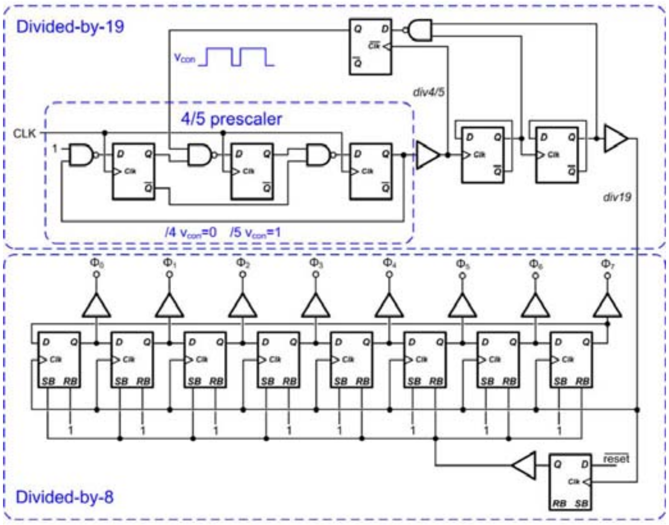
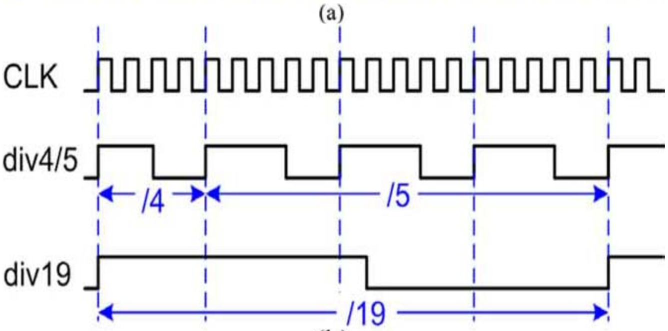


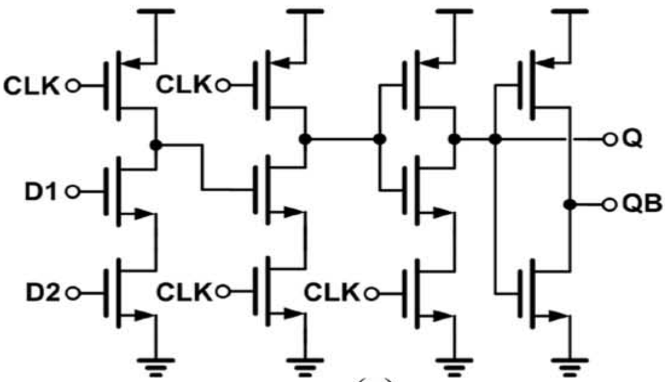
Figure 4:.Differential gm-boosted CGLNA



(a)



(b)



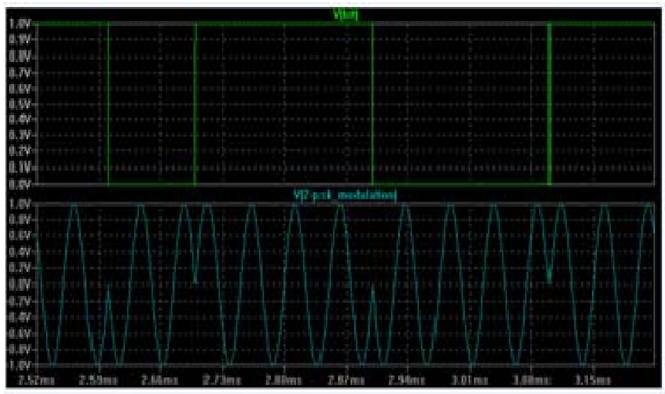
(c)

Figure 5: The architecture of: (a) feedback divider, (b) timing diagram of divided- by-19 divider, and (c) NAND gate embedded TSPC filp-flop.

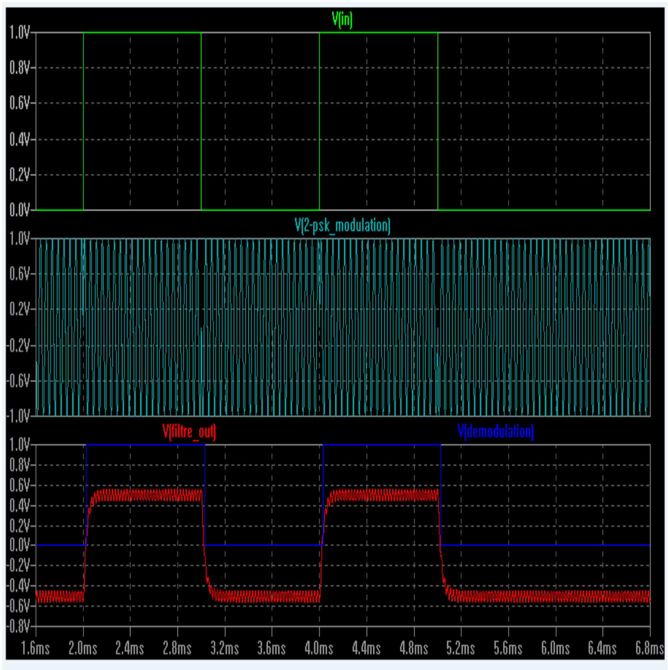
4. Experimental Results

The designed circuit is simulated using LT SPICE 1V . This being a macro design the power dissipation for the RF/analog front-end (LNA + mixer +post amplifier + channel selection filter) is about 9.6W, while the data demodulator and CRL consumes about 10.8W. The modulation signal and demodulated signal of the designed schematic at 2.432 GHz, is shown in Figure. 6. The proposed architecture can extract the carrier frequency directly from the RF signal without resort to extra resonator based reference.

The measured phase noise performance is shown in Figure. 7, which is about -91dBc/Hz at 1 MHz offset. The phase noise performance is also comparable to RF frequency synthesizer with crystal reference. Figure.8 shows the eye diagram of demodulated I/Q signal. It reveals clear eye for the data demodulation as well.



(a)



(b)

Figure 6: (a) QPSK modulated signal (b) QPSK modulated and demodulated signal.

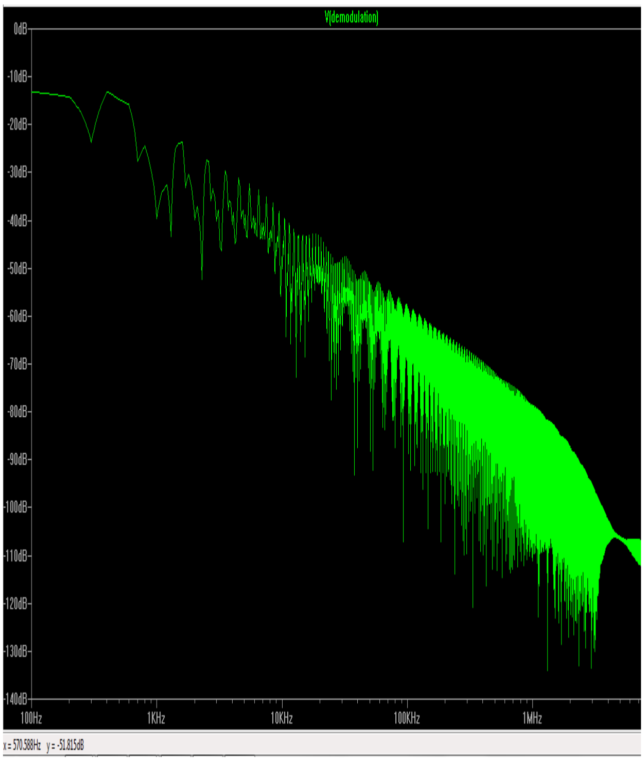


Figure7: Measured phase noise performance of recovered carrier at 2.432 GHz.

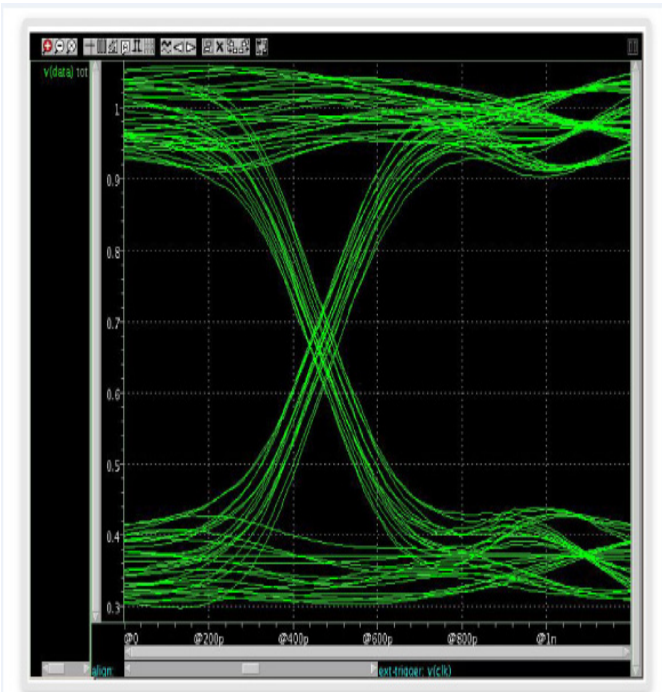


Figure 8: Measured eye diagram at QPSK demodulator output

5. Conclusion

This paper proposes a novel single chip wireless QPSK Receiver design without resort to extra resonator based reference. In contrast to conventional architectures, the receiver recovers the RF carrier frequency directly from the incident radio signal for frequency down conversion and frequency acquisition . Meanwhile, it accomplishes phase and frequency tracking as well as QPSK demodulation simultaneously. Thus no additional base-band ADCs or timing recovery loop is required in this receiver. It greatly improves the system integration level.

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