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Micro Motor Enhanced Programmable Resistance Multi Logic

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Abstract: ***In our previous work we talked about programmable resistance using PXI resistances, this programmable resistance works in 8/16/32 bits. The PRML[1] works in slow methods and which we postulate to upgrade using MEMS, The use of MEMS enhances the efficiency of the circuit , the MEMS is controlled by the program which acts much swift and we reach the result with much efficiently.***

Keywords: MEMS, Resistance Logic

1. Introduction

As the name itself claims that it is Micro Motor Enhanced **P.R.M.L[1]**, so a basic review of the previous work is essential to understand the basic concept of this paper. To recapitulate here the reduced logic into 8 steps are being discussed .This reduced logic is nothing but Universal logic reduced to only eight forms to accomplish any existing logic gate. This paper is a hypothetical approach with a concept to implement the original concept of PRML with fineness of **MEMS** replacing all the Stepper Motors as that of **PRML[1]** .In practical use of **PRML[1]** the slow stepper motors are incapable to handle the requirement of high speed data transfer in different mode , as that happens in the normal microprocessors. The **PRML[1]** profess the concept of Resistance–Resistance Logic as the basis to reduce the extra usage of **TTL** logic. Carrying the same logic concept we here have used special **MEMS** which act like a rotating switch making a contact with eight different Resistances whose values are pre-decided and which can just replace Stepper motors in **PRML[1].**

2. Circuit Concept

Micro motor Enhanced programmable device is one step ahead of Programmable Resistance Multi Logic. Here Micro motor is replacing the stepper motors for controlling the universal gate same as that of **PRML[1].** The new concept in this is a special **MEMS** encircled with 8 different valued micro resistances. The **MEMS** is having a projection which connects one resistance of pre-decided value according to the Table – I requirements. Depending on the requirement we can increase or decrease the number of **MEMS**. The greatest advantage of this device is that if we take the pre calculated resistance values with in **MEMS** we can accomplish the 8 Logic concepts by one **MEMS.** That means if we consider 8 optimum resistances within the **MEMS** we get 8 bit output directly but this needs a Nano material approach to control the resistances at such micro level. There are various software's available to programs like **COMSOL Multiphysics[2]** for making simulation of **MEMS** with minute details.

3. Schemes of the Circuit

Here two schemes has been shown as follows,

3.1 Two input and one out-put Logic.
3.2 Multi MEMS parallel Logic.

Both this schemes are a circuit design keeping various prototypes in mind and a general type is discussed here. A common Bus is taken of bits according to the requirement. In both the cases the **MEMS** are controlled by the software from outside or they are pre-decided as per the need. The

Figure 3.1

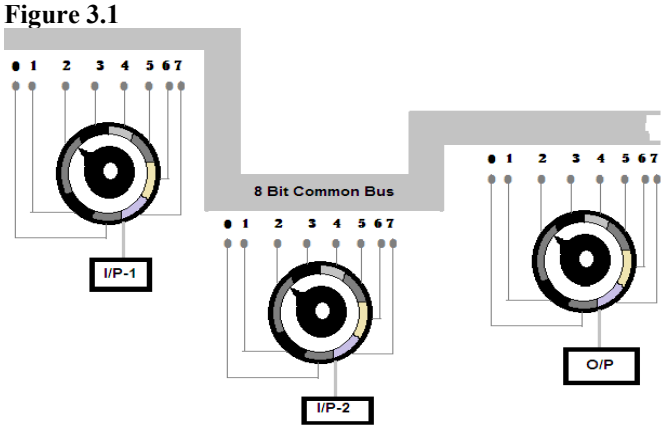
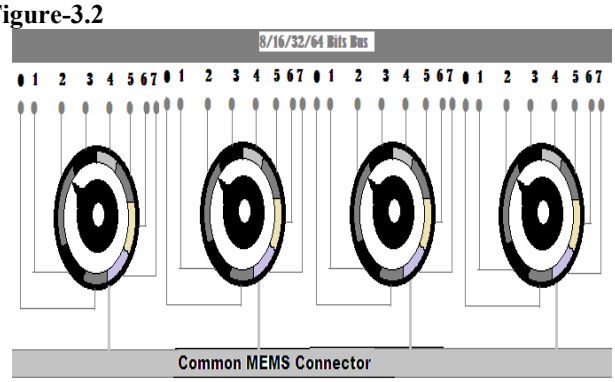


Figure 3.1: Showing Two Input and One Output Logic

Figure-3.2



Multi MEMS Parallel Logic
Figure-I
Showing four MEMS connections

Figure 3.2: Showing Multi MEMS Parallel Logic

Table 1

	A	B	O/P
1	0	0	0
2	0	1	1
3	1	0	1
4	1	1	1
5	0	1	0
6	1	0	0
7	0	0	1
8	1	1	0

The Reduced Logic Table

Table 2

R_1	R_2	R_3
L_{R11}	L_{R12}	H_{R13}
H_{R21}	L_{R22}	L_{R23}
L_{R31}	H_{R32}	L_{R33}
L_{R41}	L_{R42}	L_{R43}
H_{R71}	H_{R72}	L_{R73}

Elaborating Logic of Fig- 3.3

- L's indicate Low Resistance
- H's indicate High Resistance

Figure 3.3

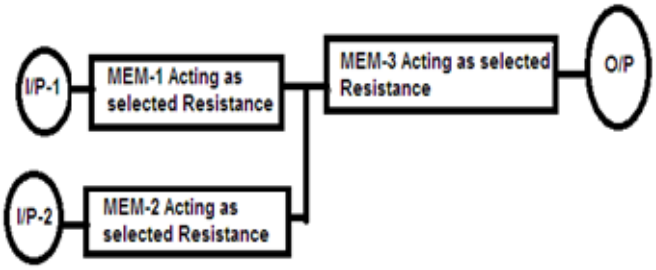


Figure 3.3: Block Diagram of two inputs and one output Logic.

whole principle rests on the concepts of Reduced logic, by saying Reduced Logic we mean to say that we took a sample of a two input and output logic circuit as shown in the Fig-3.3.In **TTL** we use transistors and diode in forward and reverse mode to make our requisite logic for which we need to change the circuit for each and every case. Till date the best we could do is the Universal Gate which is intensively used in IC's. But this lead to The Moor's law. Here we are proposing an all together new concept as that of **PRML**[1], where we are using resistances to control the Logic requirements. The most basic circuit is handled here in Fig-3.3 where two Programmable **MEMS** are used as in put and other Programmable **MEMS** is used as input. According to the Logic Requirement the **MEMS** will decide the resistance value which will direct the current to flow or not.

Under such controlled circuit situation we get the input output truth table of all the 8 reduced form as in Table- I. While opting for the pre-decided resistance value we have used Table-II which is in general form, here two types of resistances are taken H and L category. H stands for High and L stands for Low Resistance. Table-II showed the high low requirements of the circuit. One interesting development is that the reduced logic farther reduced to only five steps in practical situations. In the Table-I the first, fifth, sixth and eighth raw is having an output zero hence these are of no use in practice. Hence we are left with only five conditions for getting our all logic gate conditions in two inputs and one output mode.

3.1. Two input and one output Logic

Here the whole concept has been shown by three **MEMS**. The concept of this circuit lies in the Block Diagram of Fig-3.3 where three blocks represents three **MEMS** each having 8 inbuilt different resistances one of which is connected at a time which changes the value of the output of the resistances. Now depending on our requirement as per the resistances of Table-II we can program the MEMS.

3.2 Multi MEMS parallel Logic

Depending on the need of the system or its usage we can take 8/16/32/64 bits with the optimum Bus capacity. Here only four **MEMS** connections are being shown which can be extended to any requisite number.

4. Conclusion

As this is an enhanced concept of **PRML**[1], this circuit has got no new basic circuit concept but the main difference is the use of **MEMS** instead of stepper motors and in case of **PRML**[1] the stepper motor is controlled by embedded systems with either using Assembly language or **C** language here any of the **MEMS** control software is used instead. The **MEMS** encircled with 8 different resistances when connected by a projection the resistance value changes. There are certain chances of error if the material of the resistance is not controlled. With the use of nano material[6] the preciseness increases which can be a future aspects of this device. Another intensive analysis has to be done to manage the control of the **MEMS**. As the basis of the concept is dependent on the precise control of the **MEMS** the complicacy increases when the number of **MEMS** usage increases, when we talk about replacing the traditional **TTL** circuits by this a twofold work has to be done viz. a thorough analysis of the data transfer management and a good memory management needs to be organized with a new approach of synchronizing the both with altogether Machine Cycle concepts and applications. Another almost untouched area for development of this work is to control the heating effect to get a precise control of the device which can be done by implementing concepts of micro thermo control[4] or any other smart material where the resistivity can be dictated using by some other means as that of in the case of done with ZnO sensors[3]with various radiations of different frequency and intensity[6,5,3].This work like **PRML**[1] is still in its nascent state and still needs an interdisciplinary approach to overcome the hurdles and implement. In comparison to **PRML**[1] it more practical and more high implementable.

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