International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Impact Factor (2012): 3.358

A Survey on Low Power TSPC and E-TSPC CMOS 2/3 Prescaler

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Abstract: ***This survey paper describes dynamic circuit techniques, raising only a single-phase clock which is never inverted. The implementation of a dual-modulus prescaler using an extension of the true-single-phase-clock (TSPC) technique, the extended TSPC (E-TSPC), is discussed. The E-TSPC consists of a set of composition rules for single-phase-clock circuits employing static, dynamic, latch, data precharged, and NMOS-like CMOS blocks. The power consumption and operating frequency of the extended true single-phase clock (E-TSPC)-based frequency divider is also discussed. The short-circuit power and the switching power in the E-TSPC-based divider are discussed. A low-power divide-by-2/3 unit of a prescaler is proposed and implemented using a CMOS technology.***

Keywords: TSPC, E-TSPC, Prescaler.

1. Introduction

CMOS has been the main technology for very-large-scale integration (VLSI) system design. From the beginning to nowadays, several CMOS clock policies have been proposed. The pseudo two-phase logic was one of the earliest techniques. Later on, two-phase logic structures were proposed. The domino technique associated successfully both two-phase and dynamic CMOS circuits. With the NORA technique an extensive no-race approach for two-phase and dynamic circuits was developed. A single-phase-clock policy was introduced in [the true single-phase-clock (TSPC)]. Single-phase-clock policies are superior to the others due to the simplification of the clock distribution. They reduce the wiring costs and the number of clock-signal requirements (no problems with phase overlapping, for instance). Consequently, higher frequencies and simpler designs can be achieved.

The extended true-single-phase clock CMOS circuit technique (E-TSPC), an extension of the TSPC, consists of composition rules for single-phase circuits using static, dynamic, latch, data-precharged, and NMOS-like blocks. The composition rules enlarge the block-connection possibilities and avoid races; additionally, NMOS-like blocks enhance the technique for high-speed operations. [2]

The high-speed frequency divider is a key block in frequency synthesis. The prescaler is the most challenging part in the high-speed frequency-divider design because it operates at the highest input frequency. A dual-modulus prescaler usually consists of a divide-by-2/3 (or 4/5) unit followed by several asynchronous divide-by-2 units. The operation of the divide-by-2/3 unit at the highest input frequency makes it the bottleneck of the prescaler design. To achieve the two different division ratios, D flip-flops (DFFs) and additional logic gates, which reduce the operating frequency by introducing an additional propagation delay, are used in the unit. The power consumption of this divide-by-2/3 unit, which is the greatest portion of the total power consumption in the prescaler, significantly increases due to the power consumption of the additional components. [3]

2. Related Research

In this paper describes two dynamic circuit techniques, raising only a single-phase clock which is never inverted. This class of circuits has the advantages of simple clock distribution, small area for clock lines, reduced clock skew problems, and high speed. Several examples are demonstrated. [1] In this paper implementation of a dual-modulus prescaler using an extension of the true-single-phase-clock (TSPC) technique, the extended TSPC (E-TSPC), is presented. The E-TSPC consists of a set of composition rules for single-phase-clock circuits employing static, dynamic, latch, data precharged, and NMOS-like CMOS blocks. The composition rules, as well as the CMOS blocks, are described and discussed.[2] In this paper the power consumption and operating frequency of the extended true single-phase clock (E-TSPC)-based frequency divider is investigated. The short-circuit power and the switching power in the E-TSPC-based divider are calculated and simulated. A low-power divide-by-2/3 unit of a prescaler is proposed and implemented using a CMOS technology. Compared with the existing design, a 25% reduction of power consumption is achieved. A divide-by-8/9 dual-modulus prescaler implemented with this divide-by-2/3 unit using a 0.18- m CMOS process is capable of operating up to 4 GHz with low-power consumption. The prescaler is implemented in low-power high-resolution frequency dividers for wireless local area network applications. [3] In this paper new dynamic, semi static, and fully static single-clock CMOS latches and flip-flops are proposed. By removing the speed and power bottlenecks of the original true-single-phase clocking (TSPC) and the existing differential latches and flip-flops, both delays and power consumptions are considerably reduced. For the non-differential dynamic, the differential dynamic, the semi static, and the fully static flip-flops**,** the best reduction factors are 1.3, 2.1, 2.2, and 2.4 for delays and 1.9, 3.5, 3.4, and 6.5 for power-delay products with an average activity ratio (0.25), respectively. The total and the clocked transistor numbers are decreased. In the new differential flip-flops, clock loads are minimized and logic-related transistors are purely n-type in both n- and p-latches, giving additional speed advantage to this kind of CMOS circuits.[4] In this

paper they present a completely integrated 24GHz prescaler with programmable division ratios of /4 and /5. The prescaler uses high speed differential current mode logic. AND gates are merged with flip-flops for low power consumption and minimum gate delay. Broadband static operation up 24GHz is achieved with on-chip shunt peaking inductors in the flip-flops. A broadband output buffer is included in the circuit to drive 50Ω loads. The circuit draws 49mA from a single 1.2V supply. With a reduced supply voltage of 0.9V the maximum operating frequency of the prescaler is 22 GHz and the total power dissipation is 27mW. The circuit is manufactured in 90 nm bulk CMOS technology.[5] In this paper the design of a dual modulus prescaler 32/33 in a 0.35pm CMOS technology is presented. The prescaler is a circuit employed in high frequency synthesizer designs. In the proposed circuit the technique called Extended True Single Phase Clock (E-TSPC), an extension of the True Single Phase Clock (TSPC) technique, was applied. Additionally some new structures to double the data output rate are also employed. [6]

3. Methodology

3.1 Method-1

The proposed method based on the operation of Single-Phase Dynamic Logic and the operation of Single-Phase Precharge Logic. [1]

A divide- by-two circuit can be the effectively used in the single-phase dynamic flip-flop. This circuit can be one stage of an asynchronous binary counter. It can also be cascaded to provide division by 4, 8, etc. As it is asynchronous, it can be very fast. The circuit is comparable to a two-phase static D-flip-flop normally used as an asynchronous counter. Our circuit contains only ten transistors compared to 16 in the static flip-flop. By using less transistors in each unit the counter can be expected to operate at higher frequencies. SPICE simulations indicate operation frequencies of 180 MHz using only standard size (3 X 7 μm^2) transistors in a 3-µm CMOS process.

For the single-phase precharge logic they have chosen a serial full adder as an example. Such a circuit is very useful in high-speed signal processing applications using bit-serial arithmetic. In this paper they propose two different serial adders. In the first circuit, Fig. 1, the two inputs are concurrent. The circuit is very similar to the serial adder suggested in, using the N-P CMOS technique. Our circuit uses slightly more transistors than the N-P CMOS circuit, 37 instead of 32. Simulation using TMODS indicates that a clock frequency of 90 MHz is possible, again using standard transistors in a 3-µm process.

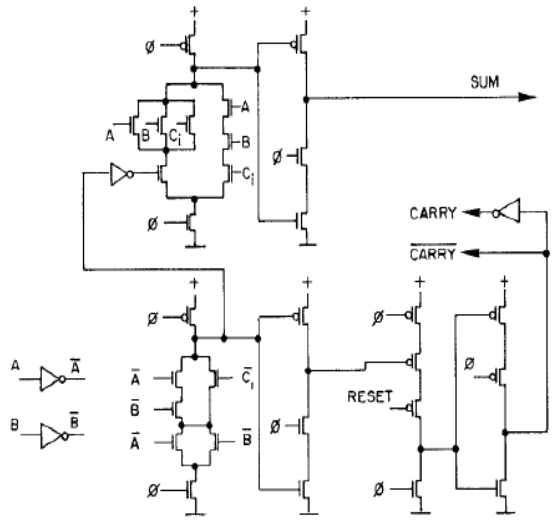

Figure 1: A serial full adder using Single-Phase-clock precharge logic and domino technique. ϕ is a Single-Phase-Clock

The second circuit, Fig. 2, is optimized for speed. This was done by never using more than three transistors in series and by limiting the logic depth to 1 for each latching instant. In this circuit input 2 is used one half periods later than input 1. The circuit contains 43 transistors. It is considerably faster than the first one. Simulation indicates that a clock frequency of 140 MHz can be used.

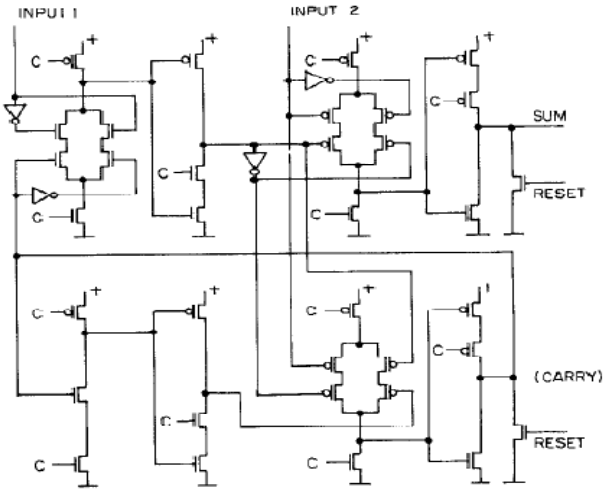

Figure 2: A serial full adder using Single-Phase-clock precharge logic optimized for speed. C is the Single-Phase clock

3.2 Method-2

This paper describes the E-TSPC circuit blocks and composition rules. It consists of four blocks such as [2]

1. Basic CMOS Blocks
2. Composition Rules
3. Exception Rule
4. NMOS-Like Logic Extension

1) Basic CMOS Blocks:
An E-TSPC circuit should use any of the blocks: CMOS static block, n-dynamic block, p-dynamic block, n-latch block, p-latch block, and high (PH) and low (PL) data-precharged blocks. The clocked transistors of the n- and p-latches are placed close to the power rail; this configuration can attain a higher speed but suffers charge sharing

problems. Clocked transistors close to either the power rail or the block output are admissible latch configurations. In data-precharged blocks, some input signals, called precharging inputs or pc-inputs, control the output precharge. If all PH block pc-inputs are high, or if all PL block pc-inputs are low, then the PH or PL block is precharged. In this case, the PH block output goes to low, and the PL block output to high.

2) Composition Rules:

First, the definition of data chains, fundamental to the design rules, is given.

Definition: An n-data chain is any non cyclic signal propagation path:

i) Containing at least one n-latch, one n-dynamic, or one n-Dp block;

ii) Starting in a circuit external input, or in the output of a p-latch, p-dynamic, or p-Dp block; when this output is followed by static blocks in the normal data flow, the data chain starts in the output of the last static block;

iii) Going through static, n-dynamic, n-Dp, or n-latch blocks;

iv) Regardless of the number and ordering of the blocks defined above;

v) Finishing in a circuit external output.

3) Exception Rule:

In consequence, the p-latch output may change during its holding time. Consider an initial state on which the signals clock, input, and output a are low, and both blocks B_{L1} and B_{L4} are evaluating. At the end of the evaluation period, the outputs a_1 and a_2 are high. Subsequently, when the clock goes to high, the other blocks will evaluate. Suppose that a_1 works properly, holding its former value (high). In this case, the node a_2 goes to low, output a goes to high, and b_1 goes to low. As a result, the transistor N_1 is cut, and the final value of node b_2 will depend on the circuit delays.

Commonly, the delay between nodes a_1 and a_2 is long enough to ensure that b_2 is fully discharged through transistors N_1 and N_2 in this case, the second D-FF works properly.

A simple exception rule is added to cover the utilization of the well-established TSPC D-FF's

Exception Rule (r_e): Configurations are similar where rules r_4 and r_5 are not obeyed, are accepted if enough delay exists. The data chains where r_e is applied, to the detriment of r_4 and r_5 do not have a latch with steady output at the holding phase. Since the correct operation of the circuit will depend on the block delays, the exception rule should be used with caution.

4) NMOS-Like Logic Extension:

When high speed is also a requirement, restrictions on the use of p-dynamic and p-latch blocks should be imposed. These Blocks have at least two p-transistors in series, which may reduce considerably the maximum speed. In such applications, the p-data chains are limited to one block, and most logic operations are handled with n-data chains with limited logic dept. Thus, deep pipelines will be necessary to implement complex and fast logic designs.

The NMOS-like blocks are faster due to the reduced number of transistors in series, but, unfortunately, they consume more power. In consequence, they should be used only in critical data chains, where the desirable speed has not been reached. Since the connection characteristics do not depend on whether it is a conventional or an NMOS-like block, the composition rules (r_1-r_5 and r_e) are valid and necessary for both; as a result, NMOS-like blocks and conventional blocks can replace one another, and the judicious selection of NMOS-like blocks is made easy.

Dual-modulus prescalers, a circuit with applications in frequency synthesis systems, have been frequently used to compare different high-speed implementations, their goal. A high-speed dual-modulus prescaler (divide by 128/129) was designed using a standard 0.8 m CMOS bulk process.

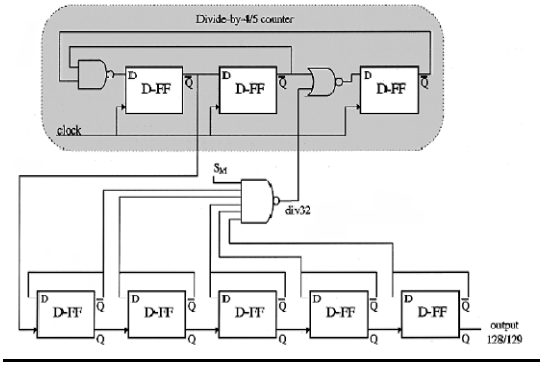

Figure 3: Schematic of the dual-modulus prescaler (divide by 128/129).

3.3 Method-3

This paper describes the TSPC AND E-TSPC DIVIDE-BY-2 UNIT [3]

1) Propagation Delay
2) Power Consumption

1) Propagation delay:

The toggled TSPC DFF is the most popular divide-by-2 unit in the high-speed frequency divider design, while the E-TSPC DFF is proposed to increase the operating frequency. When performing the divide-by-2 function, the output S3 is fed back to D.

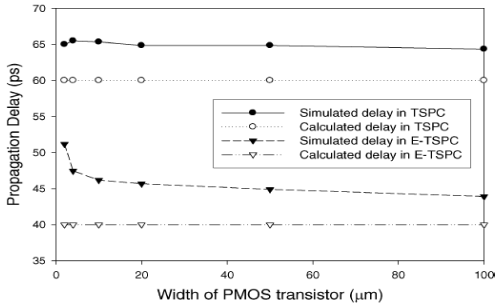

Figure 3: Propagation delay of the TSPC and E-TSPC divide-by-2 unit.2

2) Power Consumption:

By reducing the load capacitance during charging and discharging, the switching power consumption can be reduced as well. However, in the E-TSPC unit, there is a period during which a direct path from supply voltage to ground is established in the operation of divide-by-2.

4. E-TSPC-Based Prescaler

The E-TSPC divide-by-2 unit has the merit of high operating frequency compared with the traditional TSPC divide-by-2 unit. In a simplified topology of the divide-by-4/5 unit is proposed to achieve high operating frequency. To make less components work at full speed, a divide-by-2/3 is used in. Since the divide-by-2/3 unit consists of two toggle DFFs and additional logic gates, one way to effectively reduce the delay and power consumption is to integrate the logic gates to the divide-by-2/3 unit. In a gate-integrated dual-modulus prescaler based on the dynamic circuit has been proposed to achieve the high operating frequency and low power consumption. This design uses two DFFs, while the divide-by-4/5 unit in uses three DFFs. When the modulus control signal MC is logically low, it performs the divide-by-3 function. If the output of DFF2 is logically low, the node S1 of DFF2 is disabled, thus nodes S2 and S3 of DFF2 will have no switching activities, therefore, no switching power dissipation. DFF1 operates all the time, while DFF2 only operates when the output of DFF2 is logically high. When MC is logically high, the output of DFF1 will be disabled to achieve the divide-by-2 function. However, the nodes S1 and S2 of DFF1 still have switching activities since the output of DFF2 still feeds back to DFF1. Thus, both DFFs switch at half of the input frequency even if DFF1 does not participate in the divide-by-2 function. As a result, the divide-by-2 unit dissipates more power even only if one toggled DFF is needed. Such a topology introduces unnecessary power consumption, which is a significant part of the total power consumption. Moreover, during a quarter of the period, the short-circuit power still exists in DFF1.

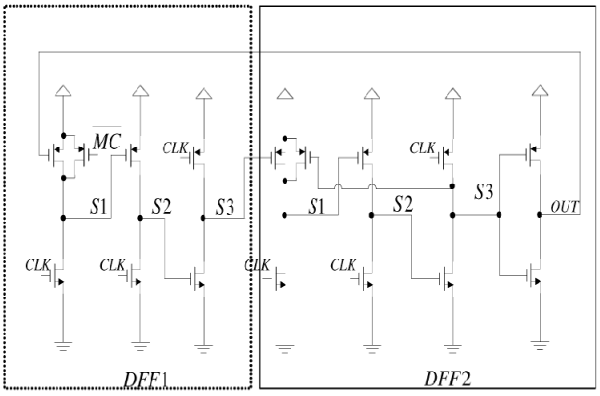

Figure 4: Proposed divide-by-2/3 unit.

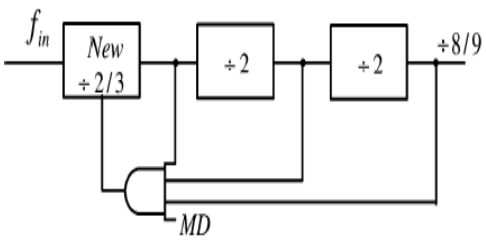

Figure 5: Topology of the divide-by-8/9 prescaler.

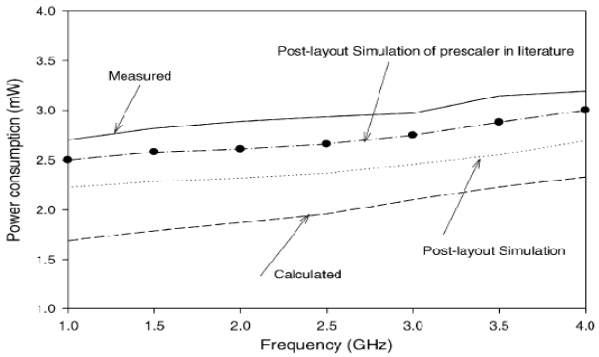

Figure 6: Power consumption of the proposed divider.

4.1 Method-4

4.1.1 Bottlenecks of the original TSPC

There are four basic stages in TSPC: precharged P- and N-stages and non-precharged (static) P- and N-stages, named PP, PN, SP, and SN stages. A positive edge-triggered flip-flop can be formed in the precharge version by a combination of PP+SP+PN+SN or, in its non-precharge version by a combination of SP+SP+SN+SN. They can call the first two stages a p-block (or p-latch) and the second two stages an n-block (or n-latch). A negative edge triggered flip-flop can be formed by exchanging the P- and N-blocks. Logic operating parts can be included in the flip-flops as long as they obey the following rules: in stages PP or PN logic parts are placed between two clocked transistor with single type transistors (p or n) and in stages SP or SN, logic parts are placed in their both ends with complementary-type transistors.

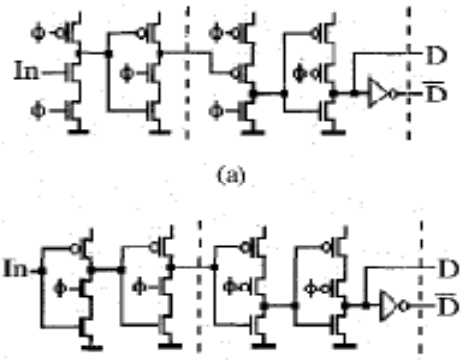

Figure 7: Complementary outputs generated from original dynamic **TSPC** flip-flops. (a) (PN + SN) + (PP + SP + INV). (b)
(SN + SN) + (SP + SP + INV).

5. A Single-Stagtes PC Full-Latch

For a non differential solution, they propose a single-stage TSPC full-latch (FL), which can latch both low and high inputs (an SP stage can only latch a low input), utilizing the available precharged-node signal. The TSPC full-latch, marked by the dash-line box, is similar to a C2MOS stage [lo] but does not need a real two-phase clock. Instead, one of the two clock inputs uses the precharged node signal of the preceding n-block. This signal has a feature of inverted clock but is data-dependent during its evaluation phase. Both p- and n-branches in the full latch now become nonconductive during the high clock phase and data-dependently conductive during the low clock phase. It works perfectly with the input data of both one and zero. There are

a number of advantages; we can mention three of them. First, the data is fully latched at the output node of the single stage, so the succeeding stage does not have to be Precharged. Second, no matter whether the succeeding stage is precharged or not, an inverter can be placed between them to generate complementary outputs. Third, the output node is a three-state node like that of a C2MOS stage, which is useful in, for example, driving a bus. Note that the critical delay path of the full-latch is the p-branch and the size of the middle n-transistor can be small, giving an insignificant load increase to the precharged node of the preceding n-block. In the case of generating complementary outputs, the overall speed is certainly improved. The preceding stage can also be a TSPC-2 type precharged n-latch (PN/SN).

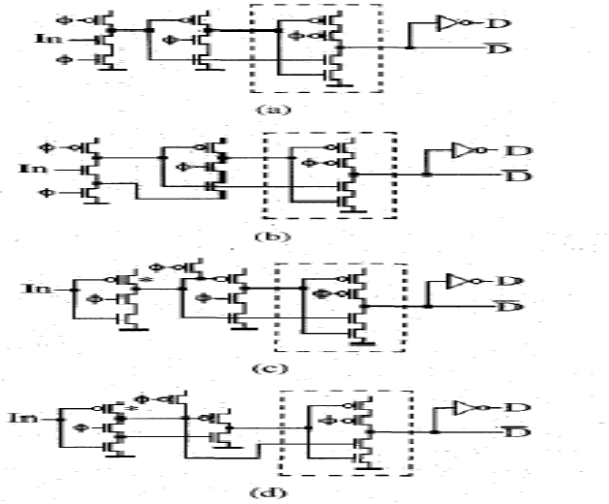

Figure 8: Complementary outputs generated from new single-clock dynamic flip-flops. (a) (PN + SN) + FL (P) + INV. (b) PN/SN + FL(P) + INV. (c) (PSN + SN) + FL(P) + INV. (d) PSLT(N) + FL(P) + INV.

6. Results

In the method-1 the simulations mentioned were done using SPICE or TMODS simulators. SPICE parameters were taken from an AMI 3-µm double-metal process (CCD process). Transistor sizes were all 3 x 7 μm^2 with a source/drain area of 7 x 8 μm^2. Timing data used in TMODS were derived from SPICE simulations using the same transistor sizes. All simulations were performed with a standard inverter as clock driver, in order to include clock slope effects.

In the method-2 the full prescaler circuit, occupying a 0.0126 mm area, was formed with the counter D_{G4}. The D-FF's of the 32 asynchronous counter were built with conventional rise edge triggered TSPC D-FF. The clock signal from the divide-by-4/5 counter is inverted before being sent to the 32 counter. This expedient allows a longer time interval for preparation of the signal div32.

Performance results of this work, of two recently published prescalers using TSPC D-FF's, and of a new prescaler architecture are summarized in Table I. Area, speed and power consumption results for four different prescalers

Table-I

prescaler	*Technology (µm)*	*Power supply (V)*	*Area ($10^3 mm^2$)*	*Speed (Ghz)*	*Power (µW/Mhz)*
[13]	1.0	5	39.1	1.6	31.2
[12]	0.8	5	13.7	1.22	20.9
[14]	0.7	5	632	1.75	13.7
(this work)	0.8	5	12.6	1.59	8.0

In the method-3 a comparison of the performances of this new divide-by-2/3 unit and the E-TSPC unit in is carried out on the grounds that the design is to achieve the best performance. The simulations are performed by using the Cadence SPECTRE RF for a 0.18- m CMOS process. The pMOS and nMOS devices of the two units are of the same size. In the divide-by-3 operation, the proposed unit has approximately 10% lower power consumption compared with that of the unit in. In the divide-by-2 operation, the proposed unit dissipates less than 40% of the power consumption of the unit in due to the former's reduced switching activities and short circuit in DFF1. If the two operations are of equal Probabilities in the dual-modulus prescaler, a 25% reduction in power consumption are achieved for the proposed unit. With an input of 4.5 GHz, the power consumption is only 790 W, while the divide-by-8/9 prescaler has a power consumption of 1.5mW for this configuration.

The input signal for the measurement is provided by the Antirust 68347C 10-MHz–20-GHz signal generator, while the output signals are captured by the Lecroy Wavemaster 8600A 6G oscilloscope. The power dissipation for the measured chip is 28 mW with the supply voltage of 1.8 V for a 4.2-GHz input in the first version because of the large size of MOS transistors. In the prescaler with smaller transistor sizes, the power consumption reduced to 3.3 mW for an input of 4 GHz at 1.8-V supply voltage.

In the method-4 To fairly compare different flip-flops, complementary outputs are always and to avoid complication in sizing, transistor widths are fixed to W, = **6** pm and W, = **3** pm except the CVSL, RAM, and STC n-latches in which W, = 4 pm and W, = **6** pm. Widths of all minimum transistors are fixed to 2 pm. Typical SPICE parameters of a 0.8-pm CMOS single-poly double-metal process are used. Three identical flip-flops are cascaded to simulate realistic input waveforms and output loads. The delay of the middle one is used. Only dynamic power consumptions are taken into account, which are calculated from node to node according to three weight factors. The first is the activity ratio A of a node.

7. Conclusion

In this paper, the concept of different methodologies has been discussed. They have demonstrated new CMOS circuit techniques, based on a true single-phase clock, where the clock is never inverted. Dynamic as well as precharged and domino circuit techniques can be used. This class of circuits uses the same or slightly more transistors than other corresponding techniques. The advantages are simple compact clock distribution and high Speed. A complete

high-speed dual-modulus prescaler (divide by 128/129) was developed in a 0.8 m CMOS process. The measured circuit attained 1.59 GHz and 8.0 mW/MHz power consumption with 5 V power supply. It can be advantageously compared with other implementations in terms of area and power consumption; in terms of speed, it matches the fastest TSPC prescaler.

The design and optimization of a high-speed E-TSPC-based prescaler has been carried out by investigation of the operating frequency and power consumption of the E-TSPC circuit. A new divide-by-2/3 unit with low power consumption has been proposed. It is suitable for the high-speed CMOS prescaler design. A divide-by-8/9 dual-modulus prescaler implemented with the proposed unit has been implemented to achieve the ultra-low-power consumption. The dual-modulus operation above 4 GHz in the TSPC-based prescaler has first been achieved. The new TSPC flip-flops speed and power bottlenecks of the original TSPC and the existing differential flip-flops are either alleviated or removed. In the best cases, delays are reduced by factors of 1.3, 2.1, 2.2, and 2.4 for the non-differential dynamic, the differential dynamic, the semi static, and the fully static flip-flops, respectively. In the same time, power consumptions are also reduced compared to their original counterparts so the power-delay products are reduced by factors of 1.9, 3.5, 3.4, and 6.5 for an average activity ratio (0.25), respectively. Particularly, the new differential dynamic, semi static and fully static flip-flops.

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