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A 1.8V 8-bit 100-MS/s Pipeline ADC in 0.18µm CMOS Technology

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Abstract: ***This paper authors have design of an 8-Bit Pipelined Analog-to-Digital Converter (ADC) which is realizing using 0.18µm CMOS technology. The simulation result is carried out in 0.18µm technology. The Supply voltage for this Pipelined ADC is ±1.8V for 0.18µm Technology. The Characterization of Pipelined ADC is done in terms of SNR, SFDR, FOM, power dissipation in 0.18µm CMOS technology. The Simulation Result shows that the Sampling Rate is 200MS/s with power Dissipation of 20.2mW was achieved in 0.18µm technology. The measured SNR is 50.2dB, SFDR is 67.56dB and FOM is 35.16 uJ/conv-step in 0.18µm Technology.***

Keywords: ADC, Dynamic charge sharing Comparator, Folded Cascade OP-AMP

1. Introduction

Analog-to-digital converters (ADCs) are very important building blocks in modem signal processing and communication systems. For signal processing, digital domain is preferred over analog domain because of its advantages such as noise immunity, storage capability, security etc. For long distance, digital communication is more reliable due to regenerative repeater. Due to these, today nearly all modern electronics are primarily digitally operated, allowing for advanced digital signal processing (DSP). But the real world signals such as signals coming from various transducers are analog in nature. This analog signal must be converted into digital to allow digital signal processing. This is done by Analog to Digital Converter (ADC) as shown in Figure 1. Similarly after signal processing in digital domain, the signal is converted back into analog. This is required for the transducer such as speaker. It is done by Digital to Analog converter (DAC). The applications of ADC include DC instruments, process control, thermocouple sensors, modems, digital radio, video signal acquisition etc. The ADC should be featured with low power and higher speed due to many reasons. First the rapid advent of battery operated portable system requires low power dissipation in order to prolong battery life, and a minimum number of battery cells to reduce the volume and weight of the system. Another reason is the smaller feature sizes offered by today's VLSI technology.

Different ADC architecture and its application are summarization in table 1. Among various ADC architectures, the pipelined ADC has the attractive feature of maintaining high accuracy at high conversion rate with low complexity and power consumption. Therefore it is used extensively in high-quality video systems, high speed data acquisition systems and high performance digital communication systems where both precision and speed are critical.

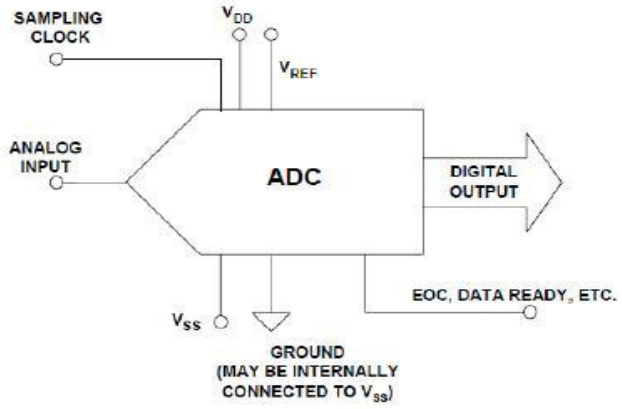

Figure 1: Ideal Block Diagram of Digital to Analog Converter

Table 1: Comparison of ADC Architectures

Architecture	*Latency*	*Speed*	*Accuracy*	*Area*
Flash	No	High	Low	High
Folding/interpolating	No	Medium-High	Low-Medium	Medium-High
Delta-Sigma	Yes	Low	High	Medium
SAR	Yes	Low	Medium-High	Low
Pipeline	Yes	Medium	Medium-High	Medium

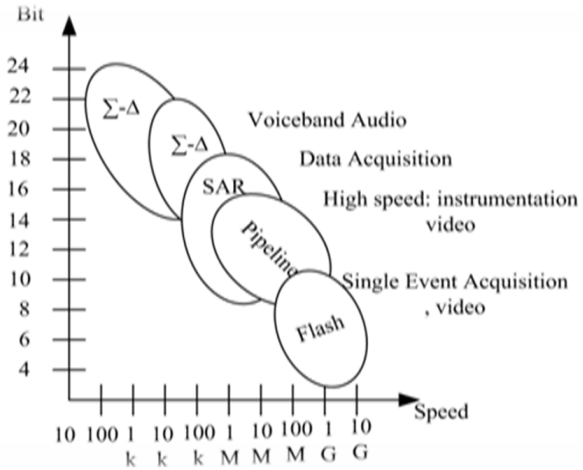

Figure 2: Various ADC Architecture

2. Architecture of Pipeline ADC

Typical pipeline architecture is illustrated in Figure 3. Each stage has the four elements of a SHA, a sub-ADC, a sub-DAC and an inter-stage gain amplifier. The operation of a single stage consists of four steps. First, the input signal is captured by the sample and hold amplifier. Second, this signal is quantized by the sub-ADC, which produces a digital output. Third, this digital signal goes to the sub-DAC which converts it to an analog signal. This analog signal is subtracted from the original sampled signal - thereby, leaving a residual signal. Fourth, this residual signal is increased to the full scale through the inter-stage amplifier. The residual signal is passed to the next stage and the procedure mentioned above is repeated.

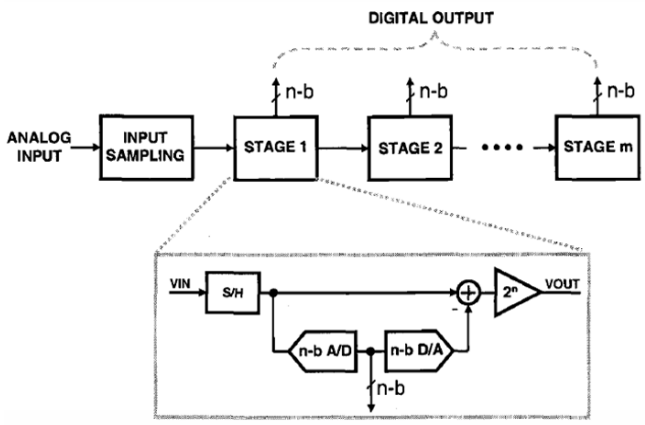

Figure 3: Generalized Pipeline ADC Architecture

3. VLSI Implementation of the 1-BIT Pipeline ADC

3.1 1- Bit Single Stage of Pipelined architecture

This stage is consist of sample and hold circuit followed by 1-bit ADC, 1-bit DAC, subtracted and multiplier. The analog signal will be sampled and fed to the comparator acts as the 1-bit ADC that would give the 1-bit digital output. Before giving to the comparator the sample signal should lift to the .9V of the DC voltage so that the comparator can compare the value to the threshold voltage and give the output. The digital output again converted to the analog value through the 1-bit DAC Uses two reference voltage levels. This converted value will be subtracted from actual sampled signal to produce an error signal using a difference circuit. This signal often called as residue signal. This residue signal again multiplied by two with an open loop amplifier. The sub tractor and the multiplier are working at 100 MS/s.

3.2 Sample and Hold Circuit

SH circuit can be realized using only a transmission gate and a capacitor. The operation of this circuit is very straightforward. Whenever CLK is high, the TG is ON, which in turn allows V_{OUT} to track V_{IN}. When CLK is low, the TG is OFF. During this time, C_H will keep V_{OUT} equal to the value of V_{IN} at the instance when CLK goes low. Implemented sample and hold is depicted in Figure 4(a).

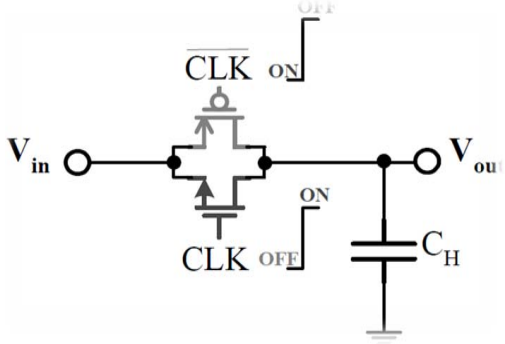

Figure 4: Schematic diagram of the sample and hold circuit

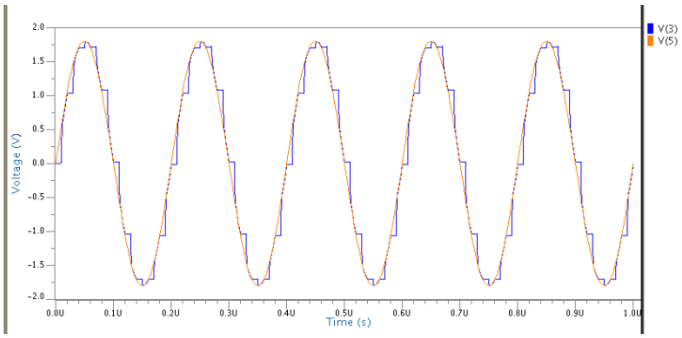

Figure 5: Simulation results of the sample and hold circuit

3.3 Design of CMOS Comparator

The Pipelined ADC consists of a 1-bit ADC which is composed of a comparator and a D-flip-flop. The design of comparator is similar enough to that of an Op-amp .The only difference is the use of the compensation network consists of resistor and capacitor and extra multipliers on a biasing NMOS device. The comparator does not need the compensation network because its only function is to switch from rail to rail. Stability is not needed as it will only slow down the switching speed. When a sine wave is input to the circuit, the comparator switches from positive rail to negative rail.

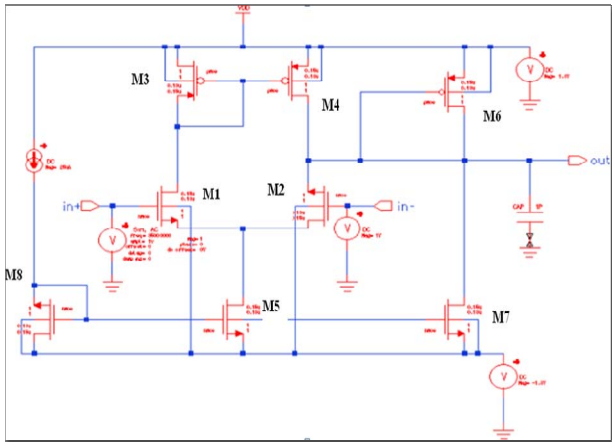

Figure 6: Schematic diagram of the comparator circuit

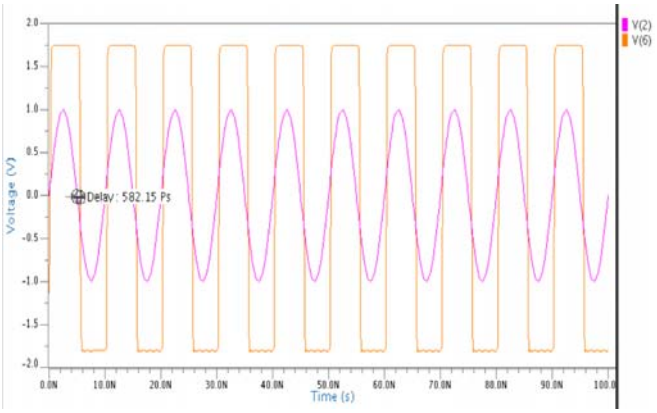

Figure 6: Simulation results of the comparator circuit

3.4 1-Bit Digital-to-Analog Converter

Basically the 1-bit DAC can be implemented using simple 2X1 analog multiplexer. Here the multiplexer has to select $\frac{Vref}{2}$ Volt or 0 Volt depending on the output of the comparator which acts as a selection line. Here in implementation of 1-bit DAC, two TGs are used as shown in Figure 6(a). Inputs to these TGs are $\frac{Vref}{2}$ and ground, while the outputs are connected together. Based on the comparator output $\frac{Vref}{2}$ or zero voltage is available at the output of DAC. The control signals for TGs are comparator output and its inverted output obtained by an inverter. In this design analog input to the DAC are 1V and 0V. Based on comparator output (+1.8V or -1.8V) one of the analog inputs will be available at the output. This is clearly observed in Figure 6(a).

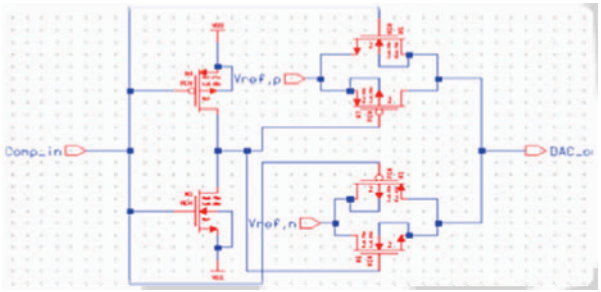

Figure 7: Schematic diagram of the 1-Bit DAC circuit

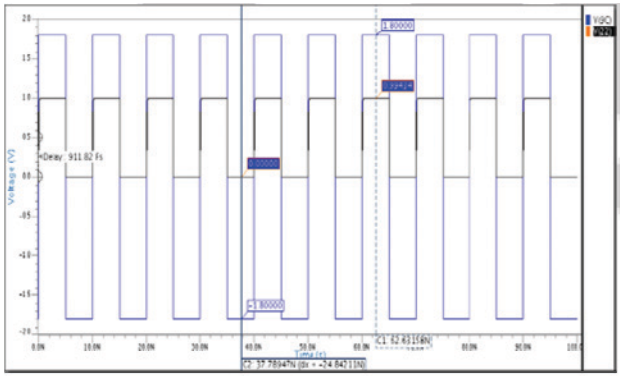

Figure 8: Simulation Result of the 1-Bit DAC circuit

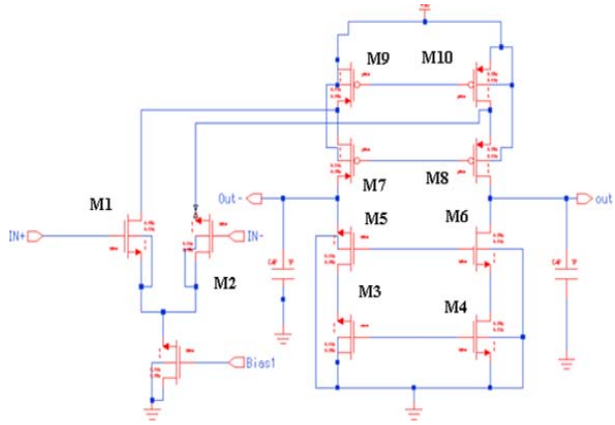

Figure 9: Schematic diagram of the Folded Cascade OPAMP circuit

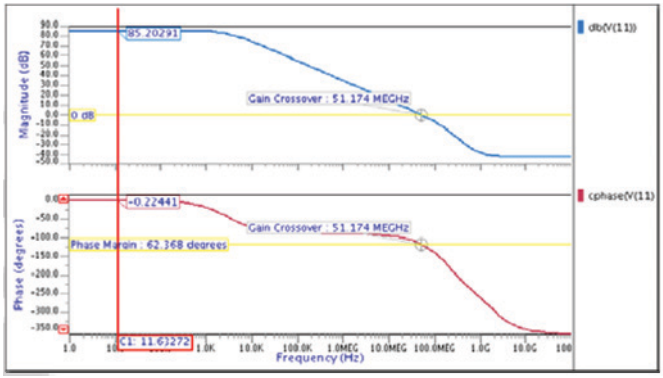

Figure 10: Frequency Response of Folded Cascade OPAMP

The circuit design of sample and hold, Comparator and DAC Op- amp, for 1-bit Pipeline ADC have been developed and implemented by using 0.18um CMOS Technology.

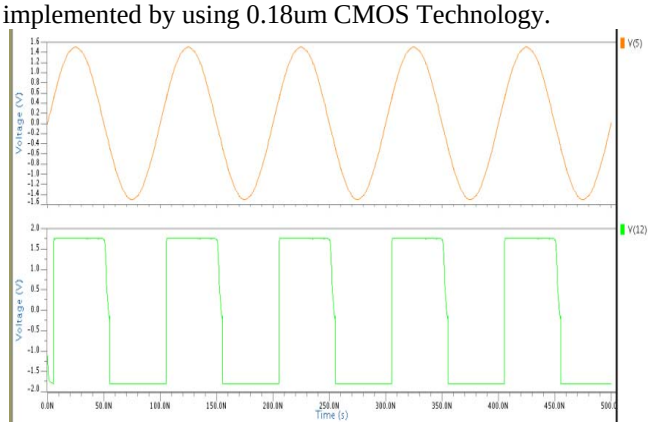

Figure 11: 1-bit Pipeline ADC output

3.5 Waveform of 8-BIT Pipelined ADC

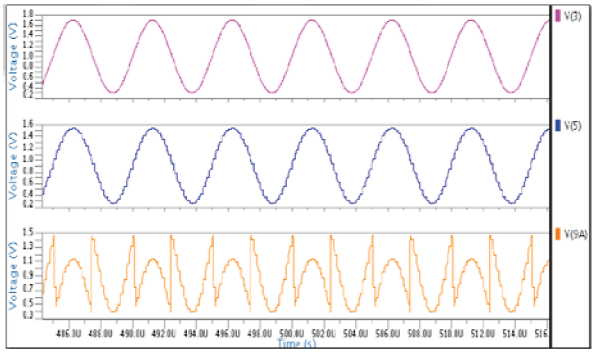

Figure 12: Residue Simulation Result of the single stage Pipelined ADC

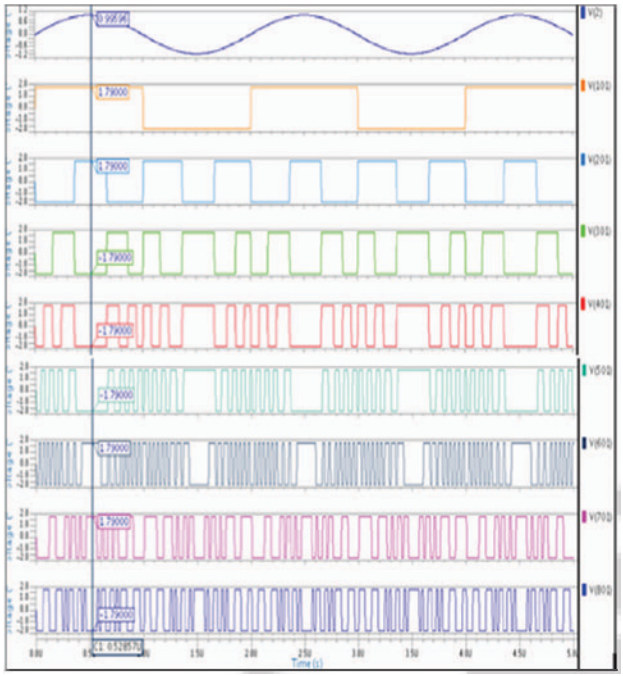

Figure 13: 8-bit Digital Output of Pipelined ADC for Analog Input

The whole 8-bit Pipeline ADC subsystem works very well under the following conditions.

Table 2: Different measured parameter in 180nm

Parameter	Value
Power supply(V)	1.8v
Input frequency(MHz)	10
Opamp Gain(dB)	60
Power dissipation(mW)	2.806

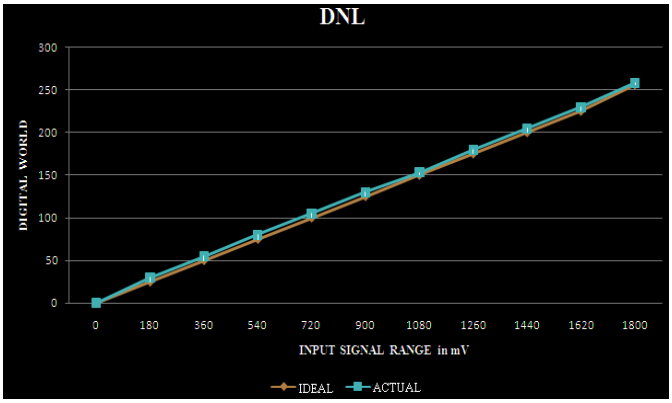

Figure 14: Measured DNL

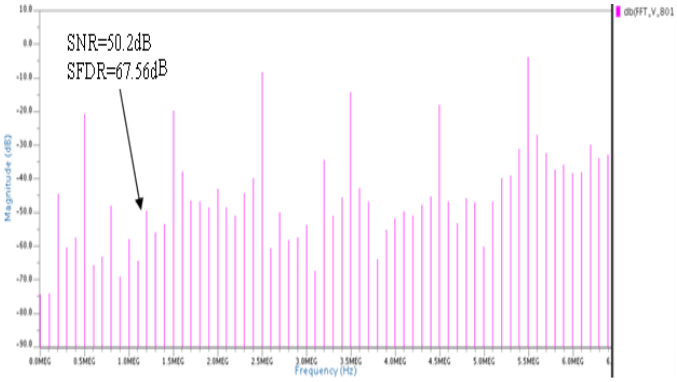

Figure 15: Measured SNR and SFDR

4. Conclusions

In this paper, a high-linearity pipelined ADC with Dynamic charge sharing Comparator in a combined front-end of the S/H and the MDAC is presented. The input signal S/H function is combined into the first MDAC using an OPAMP, achieving high power efficiency and maintaining high linearity over a large input frequency range Implemented in a 0.18µm- CMOS process, the Characteristic of Pipelined ADC is measured DNL and INL of 0.3 LSB and 0.5 LSB, respectively. The prototype ADC achieves 67.56-dB SFDR and 50.2-dB SNR at a 200-MS/s sampling rate with a 100-MHz input signal. The ADC consumes 20.3mWunder a 1.8-V supply, demonstrating a FOM of 35.16 uJ/conv-step

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