

Design of Parallel Linear Phase FIR Digital Filter of Odd Length based on Fast FIR Algorithm

Md Raju Ali¹, Jobbin Abraham Ben²

¹M.Tech VLSI Design, Department of Electronics and Communication Engineering, Hindustan University, Chennai, India

²Assistant Professor, Department of Electronics and Communication Engineering, Hindustan University, Chennai, India

Abstract: Based on published Area efficient VLSI implementation for parallel linear phase FIR digital filter of odd length based on fast FIR algorithm, this paper proposes a parallel FIR filter structure with less hardware complexity. In previous paper using carry save adder are replaced by ripple carry adder which can reduce the area.

Keywords: Fast FIR algorithms (FFA), ripple carry adder (RCA), carry save adder (CSA), symmetric convolution.

1. Introduction

The demand of high performance and low power digital signal processing (DSP) is getting higher and higher in multimedia application. The FIR filter one of device which performed in DSP system, ranging from wireless communication to video and image processing. Some application need to operate fir filter at high frequency such as video processing and other need high throughput with low power such as multiple-input multiple-output. In brief here, parallel FIR digital filter will be discussed. Because its linear increase in hardware implementation cost will increase because of increasing the block size L, there is few papers success to reduced the complexity of the fir filter [1]-[11]. In this the first [1]-[4] using polyphase decomposition, by cascading or iterating constructed first the small sized and then larger block sized parallel fir filter. In [1]-[3] using FFA they implemented L parallel filter using (2L-1) subfilter blocks which length is N/L. Using this FFA, it can reduces the required number of multipliers. The fast linear convolution is used to develop the small sized filtering structures and then a long convolution is decomposed into several short convolution in paper [5]- [9].

In [10], they designed for symmetric convolution based on even length and in [11] based on odd length. In both they are using carry save adder, but we can show that by using ripple carry adder we can reduce the area. The brief is organized as follows, introduction of FFA is reviewed in section 2, the proposed parallel FIR filter architecture are presented in section 3, and in section 4 the conclusion is given.

2. FFA

The general form of an N-tap FIR filter can expressed as

$$y(n) = \sum_{i=0}^{N-1} h(i)x(n-i), n = 0, 1, 2, \dots, \infty (1)$$

where x(n) = input sequence of infinite length and h(i) = filter coefficients. As [3], the L-parallel FIR filter can be derived using polyphase decomposition.

$$\sum_{p=0}^{L-1} Y_p(z^L)z^{-p} = \sum_{q=0}^{L-1} X_q(z^L)z^{-p} \sum_{r=0}^{L-1} H_r(z^L)z^{-r}$$

Where (2)

$$X_q(z) = \sum_{k=0}^{\alpha} z^{-k} x(LK + q)$$

$$H_r(z) = \sum_{k=0}^{\frac{N-1}{L}-1} z^{-k} h(LK + r)$$

And

$$Y_p(z) = \sum_{k=0}^{\alpha} z^{-k} y(LK + p)$$

2.1 3 × 3 FFA

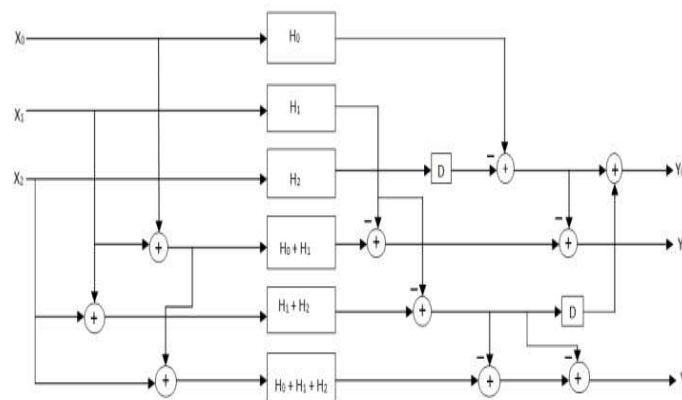


Figure 1: Three parallel FIR filter implementation using the FFA.

As [1], [3] a three parallel FIR filter using FFA can expressed as

$$Y_0 = H_0 X_0 - z^{-3} H_2 X_2 + z^{-3} [(H_1 + H_2)(X_1 + X_2) - H_1 X_1]$$

$$Y_1 = [(H_0 + H_2)(X_0 + X_2) - H_1 X_1] - [H_0 X_0 - z^{-3} H_2 X_2]$$

$$Y_2 = [(H_0 + H_1 + H_2)(X_0 + X_1 + X_2)] - [(H_0 + H_1)(X_0 + X_1) - H_1 X_1] - [(H_1 + H_2)(X_1 + X_2) - H_1 X_1] (3)$$

The implementation from (3) is shown fig. 1.

3. Proposed structure

The new three parallel FIR filter structure are proposed, which enables more multipliers sharing in the subfilter section and therefore can save more hardware cost.

1) Proposed structure 3A using RCA, ((N mod 3=0))

In odd length N for a symmetric coefficients, when (N mod 3 = 0), (4) which is presented from (3) can earn two more subfilter block which containing symmetric coefficients as [11], by using ripple carry adder we can reduce the area. The implementation is shown in fig. 2. and the Comparison of Subfilter between Existing FFA and the proposed structure 3A is shown fig.3.

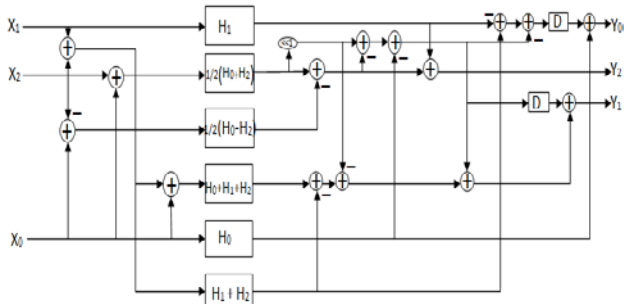


Figure 2: Implementation of the proposed structure 3A.

Existing FFA	Proposed 3A
H_0	H_1
H_1	$\frac{1}{2}(H_0 + H_2)$
H_2	$\frac{1}{2}(H_0 - H_2)$
$H_0 + H_1$	$H_0 + H_1 + H_2$
$H_1 + H_2$	H_0
$H_0 + H_1 + H_2$	$H_1 + H_2$

Figure 3: Comparison of Subfilter between Existing FFA and proposed structure 3A.

$$Y_0 = H_0 X_0 + z^{-3} \left\{ (H_1 + H_2)(X_1 + X_2) - (H_1 - H_2)(X_1 - X_2) \right\}$$

$$Y_1 = (H_0 + H_1 + H_2)(X_0 + X_1 + X_2) - (H_1 + H_2)(X_1 + X_2) - (H_0 + H_2)(X_0 + X_2) + \frac{1}{2} \left[(H_0 + H_2)(X_0 + X_2) - (H_0 - H_2)(X_0 - X_2) \right] - H_0 X_0 + z^{-3} \left\{ (H_0 + H_2)(X_0 + X_2) - (H_0 - H_2)(X_0 - X_2) \right\} - H_0 X_0$$

$$Y_2 = H_1 X_1 + \frac{1}{2} \left[(H_0 + H_2)(X_0 + X_2) - (H_0 - H_2)(X_0 - X_2) \right] \quad (4)$$

After applying the proposed structure in figure 2, the proposed system can save area.

2). Proposed structure 3B with RCA, ((N mod 3=1)).

In odd length N for a symmetric coefficients, when (N mod 3 = 1), which is presented in (5) can earn one more subfilter block which containing symmetric coefficients as [11], by

using ripple carry adder we can reduce the area. The implementation is shown in fig.4. and the comparison of Subfilter between Existing FFA and the proposed structure

3B is shown fig.5.

$$Y_0 = H_0 X_0 + z^{-3} \left\{ \frac{1}{2} (H_1 + H_2)(X_1 + X_2) - (H_1 - H_2)(X_1 - X_2) \right\}$$

$$Y_1 = (H_0 + H_1 + H_2)(X_0 + X_1 + X_2) - (H_1 + H_2)(X_1 + X_2) - (H_0 + H_1)(X_0 + X_1) + \frac{1}{2} \left[(H_1 + H_2)(X_1 + X_2) - (H_1 - H_2)(X_1 - X_2) \right] - H_2 X_2 + z^{-3} H_2 X_2$$

$$Y_2 = (H_0 + H_1 + H_2)(X_0 + X_1 + X_2) - (H_1 + H_2)(X_1 + X_2) - (H_0 + H_1)(X_0 + X_1) + 2 \left[(H_1 + H_2)(X_1 + X_2) - (H_1 - H_2)(X_1 - X_2) \right] - H_2 X_2 \quad (5)$$

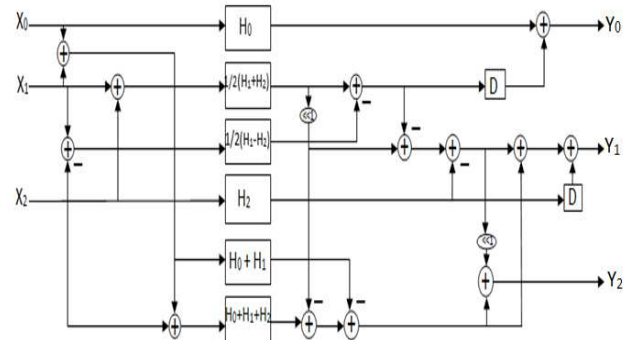


Figure 4: Implementation of the proposed structure 3B

Existing FFA	Proposed 3B
H_0	H_1
H_1	$\frac{1}{2}(H_1 + H_2)$
H_2	$\frac{1}{2}(H_1 - H_2)$
$H_0 + H_1$	H_2
$H_1 + H_2$	$H_0 + H_1$
$H_0 + H_1 + H_2$	$H_0 + H_1 + H_2$

Figure 5: Comparison of Subfilter between Existing FFA and proposed structure 3B

3) Proposed structure 3C with RCA ((N mod 3 = 2)).

In odd length N for a symmetric coefficients, when (N mod 3 = 2), which is presented in (6) can earn one more subfilter block which containing symmetric coefficients as [11], by using ripple carry adder we can reduce the area. The implementation is shown in fig. 6 and the Comparison of Subfilter between Existing FFA and the proposed structure 3C is shown fig.7.

$$Y_0 = (H_0 + H_1)(X_0 + X_1) - \frac{1}{2} \left[(H_0 + H_1)(X_0 + X_1) - (H_0 - H_1)(X_0 - X_1) \right] - H_1 X_1 + z^{-3} \left\{ (H_0 + H_1 + H_2)(X_0 + X_1 + X_2) - (H_0 + H_1)(X_0 + X_1) - \left[(H_0 + H_2)(X_0 + X_2) - (H_0 + H_1)(X_0 + X_1) \right] - \frac{1}{2} \left[(H_0 + H_1)(X_0 + X_1) - (H_0 - H_1)(X_0 - X_1) \right] - H_1 X_1 \right\}$$

$$Y_1 = \frac{1}{2} \left[(H_0 + H_1)(X_0 + X_1) - (H_0 - H_1)(X_0 - X_1) \right] + z^{-3} H_2 X_2$$

$$Y_2 = H_1 X_1 + \left\{ (H_0 + H_2)(X_0 + X_2) - \left[(H_0 + H_1)(X_0 + X_1) - \frac{1}{2} \left[(H_0 + H_1)(X_0 + X_1) - (H_0 - H_1)(X_0 - X_1) \right] \right] - H_1 X_1 \right\} - H_2 X_2 \quad (6)$$

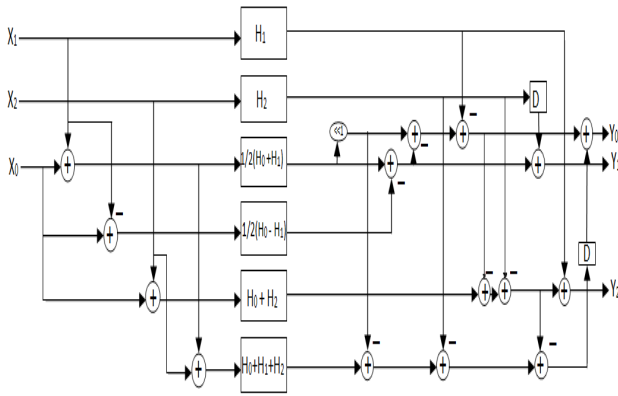


Figure 6: Implementation of the proposed structure 3C

Existing FFA	Proposed 3C
H_0	H_1
H_1	H_2
H_2	$\frac{1}{2}(H_0 + H_1)$
$H_0 + H_1$	$\frac{1}{2}(H_0 - H_1)$
$H_1 + H_2$	$H_0 + H_2$
$H_0 + H_1 + H_2$	$H_0 + H_1 + H_2$

Figure 7: Comparison of Subfilter between Existing FFA and proposed structure 3C

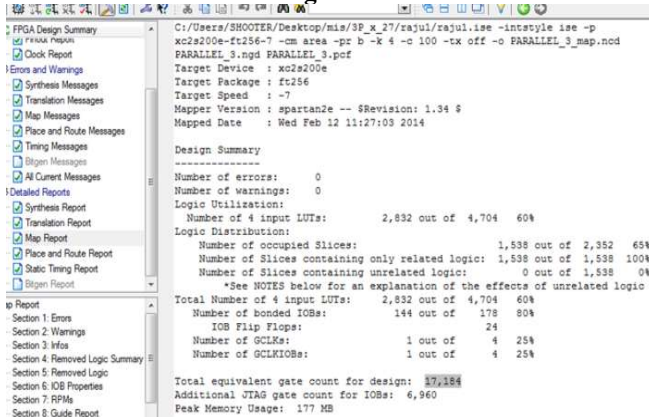
A comparison between the existing FFA and the Proposed FFA is shown in Table 1 below

Table 1: Synthesis results for Three parallel 27 tap FIR filter

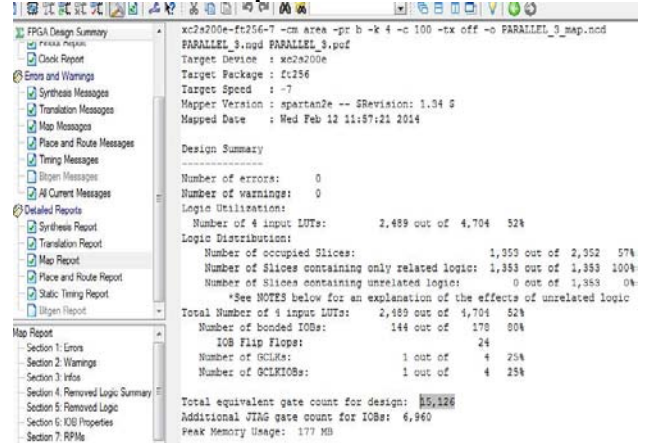
Structure	CSA(Existing)	CA(Proposed)
3-parallelFIR filter	17184	15124
FIR filter 3A	17133	14799
FIR filter 3B	16055	13794
FIR filter 3C	14841	12942

Simulation Results for comparing the existing and proposed structure is given below

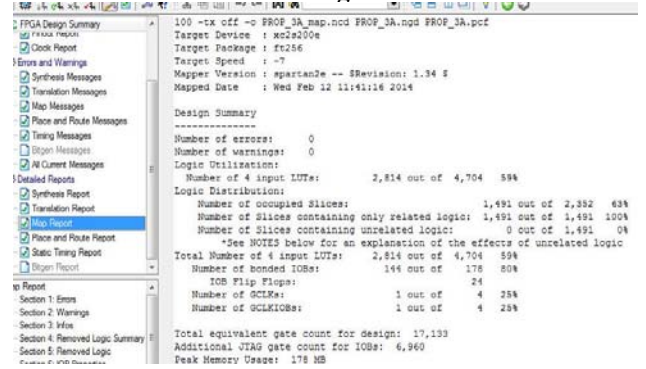
Existing FIR filter



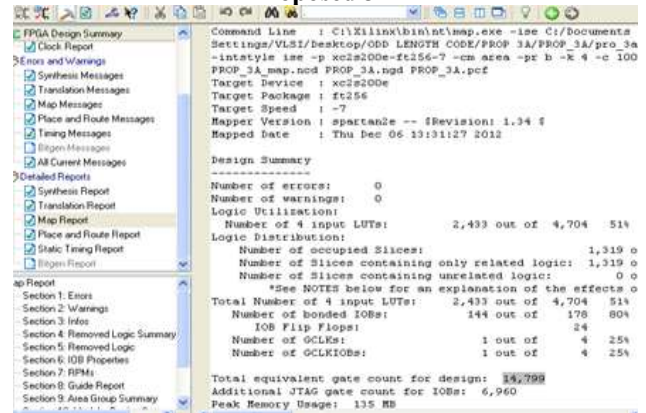
Proposed FIR filter



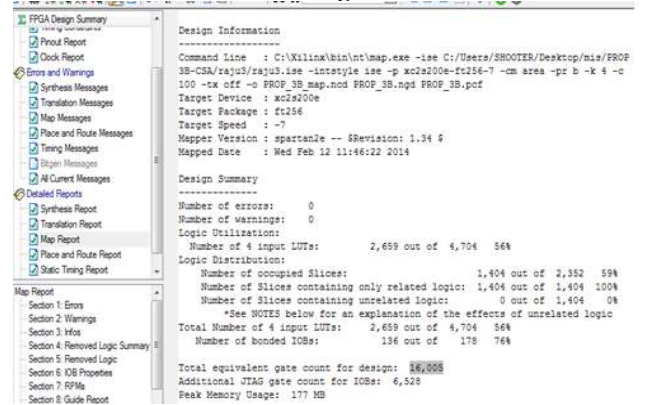
Existing 3A



Proposed 3A



Existing 3B



Proposed 3B

Design Summary	
Number of errors:	0
Number of warnings:	0
Logic Utilization:	
Number of Slice Flip Flops:	24 out of 13,824 1%
Number of 4 input LUTs:	2,267 out of 13,824 16%
Logic Distribution:	
Number of occupied Slices:	1,235 out
Number of Slices containing only related logic:	1,235 out
Number of Slices containing unrelated logic:	0 out
*See NOTES below for an explanation of the effects of	
Total Number of 4 input LUTs:	2,267 out of 13,824 16%
Number of bonded IOBs:	136 out of 325 41%
Number of GCLNs:	1 out of 4 25%
Number of GCLKIOBs:	1 out of 4 25%
Total equivalent gate count for design: 13,794	
Additional JTAG gate count for IOBs: 6,576	
Peak Memory Usage: 146 MB	

Existing 3C

Design Summary	
Number of errors:	0
Number of warnings:	0
Logic Utilization:	
Number of 4 input LUTs:	2,465 out of 4,704 52%
Logic Distribution:	
Number of occupied Slices:	1,304 out of 2,352 55%
Number of Slices containing only related logic:	1,304 out of 1,304 100%
Number of Slices containing unrelated logic:	0 out of 1,304 0%
*See NOTES below for an explanation of the effects of unrelated logic	
Total Number of 4 input LUTs:	2,465 out of 4,704 52%
Number of bonded IOBs:	128 out of 178 71%
Total equivalent gate count for design: 8,884	
Additional JTAG gate count for IOBs: 6,144	

Proposed 3C

Design Summary	
Number of errors:	0
Number of warnings:	0
Logic Utilization:	
Number of Slice Flip Flops:	24 out of 13,824 1%
Number of 4 input LUTs:	2,124 out of 13,824 15%
Logic Distribution:	
Number of occupied Slices:	1,147 out
Number of Slices containing only related logic:	1,147 out
Number of Slices containing unrelated logic:	0 out
*See NOTES below for an explanation of the effects of	
Total Number of 4 input LUTs:	2,124 out of 13,824 15%
Number of bonded IOBs:	128 out of 510 25%
Number of GCLNs:	1 out of 4 25%
Number of GCLKIOBs:	1 out of 4 25%
Total equivalent gate count for design: 12,944	
Additional JTAG gate count for IOBs: 6,192	
Peak Memory Usage: 146 MB	

4. Conclusion

In this paper we have brief, we have presented the parallel FIR structure which is reduced the area. Multipliers are major component which we can be replaced by using the fast FIR algorithm. In this paper we presented ripple carry adder in the odd length instead of carry save adder.

5. Future Scope

The future scope of this project lies in the further optimization of area and as well as power.

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Author Profile

Md.Raju Ali received his B.Tech. degree in Electronics and Communication Engineering from North Eastern Hill University, Meghalaya, India and undergoing M.Tech Degree in VLSI Design in Hindustan University, Chennai, Tamil Nadu, India. His area of interest is in design of electronic circuits.

Jobbin Abraham Ben received his B.E. degree in Instrumentation and Control Engineering from Sadar Vallabhai Patel Institute of technology, Gujarat University Vasat, India. He obtained his M.E. degree in VLSI design from K.C.G. College of technology, Karappakam Chennai, Tamilnadu, India. Currently he is an Assistant Professor in the department of Electronics and Communication Engineering, Hindustan Institute of Technology and Science, Chennai, India.