Design of Parallel Linear Phase FIR Digital Filter of Odd Length based on Fast FIR Algorithm

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Abstract: Based on published Area efficient VLSI implementation for parallel linear phase FIR digital filter of odd length based on fast FIR algorithm, this paper proposes a parallel FIR filter structure with less hardware complexity. In previous paper using carry save adder are replaced by ripple carry adder which can reduce the area.

Keywords: Fast FIR algorithms (FFA), ripple carry adder (RCA), carry save adder (CSA), symmetric convolution.

1. Introduction

The demand of high performance and low power digital signal processing (DSP) is getting higher and higher in multimedia application. The FIR filter one of device which performed in DSP system, ranging from wireless communication to video and image processing. Some application need to operate fir filter at high frequency such as video processing and other need high throughout with low power such as multiple-input multiple-output. In brief here, parallel FIR digital filter will be discussed. Because its linear increase in hardware implementation cost will increase because of increasing the block size L, there is few papers success to reduced the complexity of the fir filter [1]-[11]. In this the first [1]-[4] using polyphase decomposition, by cascading or iterating constructed first the small sized and then larger block sized parallel fir filter. In [1]-[3] using FFA they implemented L parallel filter using (2L-1) subfilter blocks which length is N/L. Using this FFA, it can reduces the required number of multipliers. The fast linear convolution is used to develop the small sized filtering structures and then a long convolution is decomposed into several short convolution in paper [5]- [9].

In [10], they designed for symmetric convolution based on even length and in [11] based on odd length. In both they are using carry save adder, but we can show that by using ripple carry adder we can reduce the area. The brief is organized as follows, introduction of FFA is reviewed in section 2, the proposed parallel FIR filter architecture are presented in section 3,and in section 4 the conclusion is given.

2. FFA

The general form of an N-tap FIR filter can expressed as

$$y(n) = \sum_{i=0}^{N-1} h(i) x(n-i), n = 0, 1, 2, ..., \infty (1)$$

where x(n) = input sequence of infinite length and h(i) = filter coefficients. As [3], the L-parallel FIR filter can be derived using polyphase decomposition.

$$\sum_{p=0}^{L-1} Y_p(z^L) z^{-p} = \sum_{q=0}^{L-1} X_q(z^L) z^{-p} \sum_{r=0}^{L-1} H_r(z^L) z^{-r}$$

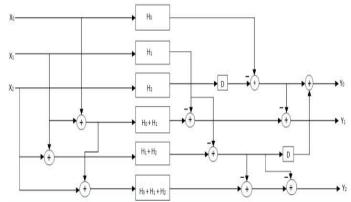
Where (2)

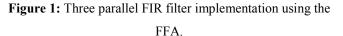
$$X_{q}(z) = \sum_{k=0}^{u} z^{-k} x (LK + q)$$
$$H_{r}(z) = \sum_{k=0}^{\frac{N}{L}-1} z^{-k} h (LK + r)$$

And

$$Y_{p}(z) = \sum_{k=0}^{\alpha} z^{-k} y(LK + p)$$

2.1 3 ×3 FFA





As [1], [3] a three parallel FIR filter using FFA can expressed as

 $\begin{aligned} Y_0 &= H_0 X_0 - z^{-3} H_2 X_2 + z^{-3} [(H_1 + H_2)(X_1 + X_2) - H_1 X_1] \\ Y_1 &= [(H_0 + H_2)(X_0 + X_2) - H_1 X_1] - [H_0 X_0 - z^{-3} H_2 X_2] \\ Y_2 &= [(H_0 + H_1 + H_2)(X_0 + X_1 + X_2)] - [(H_0 + H_1)(X_0 + X_1) - H_1 X_1] \\ &- [(H_1 + H_2)(X_1 + X_2) - H_1 X_1] (3) \end{aligned}$

The implementation from (3) is shown fig. 1.

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3. Proposed structure

The new three parallel FIR filter structure are proposed, which enables more multipliers sharing in the subfilter section and therefore can save more hardware cost.

1) Proposed structure 3A using RCA,((N mod 3=0))

In odd length N for a symmetric coefficients, when (N mod 3 = 0), (4) which is presented from (3) can earn two more subfilter block which containing symmetric coefficients as [11],by using ripple carry adder we can reduce the area. The implementation is shown in fig. 2. and the Comparison of Subfilter between Existing FFA and the proposed structure 3A is shown fig.3.

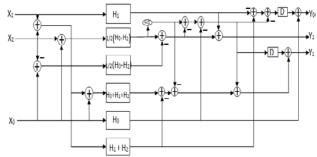


Figure 2: Implementation of the proposed structure 3A.

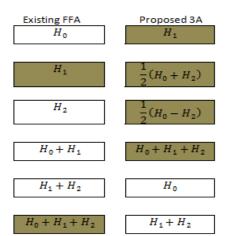


Figure 3: Comparison of Subfilter between Existing FFA and proposed structure 3A.

$$\begin{split} Y_{0} &= H_{0}X_{0} + z^{-3} \Biggl\{ (H_{1} + H_{2})(X_{1} + X_{2}) - H_{1}X_{1} - \Biggl((H_{0} + H_{2})(X_{0} + X_{2}) - H_{0}X_{0} - \frac{1}{2} [[H_{0} + H_{2})(X_{0} + X_{2}) - (H_{0} - H_{2})(X_{0} - X_{2})]] \Biggr\} \Biggr\} \\ Y_{1} &= (H_{0} + H_{1} + H_{2})(X_{0} + X_{1} + X_{2}) - (H_{1} + H_{2})(X_{1} + X_{2}) - (H_{0} + H_{2})(X_{0} + X_{2}) + \Biggl\{ (H_{0} + H_{2})(X_{0} + X_{2}) - \frac{1}{2} \Biggr\} \\ \times [(H_{0} + H_{2})(X_{0} + X_{2}) - (H_{0} - H_{2})(X_{0} - X_{2})] - H_{0}X_{0} \Biggr\} + z^{-3} \Biggl\{ (H_{0} + H_{2})(X_{0} + X_{2}) - \frac{1}{2} [(H_{0} + H_{2})(X_{0} + X_{2}) - (H_{0} - H_{2})(X_{0} - X_{2})] - (H_{0} - H_{2})(X_{0} - X_{2})] - H_{0}X_{0} \Biggr\} \\ Y_{2} &= H_{1}X_{1} + \frac{1}{2} [(H_{0} + H_{2})(X_{0} + X_{2}) - (H_{0} - H_{2})(X_{0} - X_{2})] \Biggr\} \Biggr\}$$

After applying the proposed structure in figure 2, the proposed system can save area.

2). Proposed structure 3B with RCA,((N mod 3=1)).

In odd length N for a symmetric coefficients, when (N mod 3 = 1), which is presented in (5) can earn one more subfilter block which containing symmetric coefficients as [11], by

using ripple carry adder we can reduce the area. The implementation is shown in fig.4. and the comparison of Subfilter between Existing FFA and the proposed structure

3B is shown fig.5.

 $Y_{0} = H_{0}X_{0} + z^{-3} \left\{ \frac{1}{2} (H_{1} + H_{2})(X_{1} + X_{2}) - (H_{1} - H_{2})(X_{1} - X_{2}) \right\}$ $Y_{1} = (H_{0} + H_{1} + H_{2})(X_{0} + X_{1} + X_{2}) - (H_{1} + H_{2})(X_{1} + X_{2}) - (H_{0} + H_{1})(X_{0} + X_{1}) + [(H_{1} + H_{2})(X_{1} + X_{2}) - \frac{1}{2}$ $\times [(H_{1} + H_{2})(X_{1} + X_{2}) - (H_{1} - H_{2})(X_{1} - X_{2})] - H_{2}X_{2}] + z^{-3}H_{2}X_{2}$ $Y_{2} = (H_{0} + H_{1} + H_{2})(X_{0} + X_{1} + X_{2}) - (H_{1} + H_{2})(X_{1} + X_{2}) - (H_{0} + H_{1})(X_{0} + X_{1}) + 2[(H_{1} + H_{2})(X_{1} + X_{2}) - \frac{1}{2}$ $\times [(H_{1} + H_{2})(X_{1} + X_{2}) - (H_{1} - H_{2})(X_{1} - X_{2})] - H_{2}X_{2}] + z^{-3}H_{2}X_{2}$ $Y_{2} = (H_{0} + H_{1} + H_{2})(X_{0} + X_{1} + X_{2}) - (H_{1} + H_{2})(X_{1} + X_{2}) - (H_{0} + H_{1})(X_{0} + X_{1}) + 2[(H_{1} + H_{2})(X_{1} + X_{2}) - \frac{1}{2}$ $\times [(H_{1} + H_{2})(X_{1} + X_{2}) - (H_{1} - H_{2})(X_{1} - X_{2})] - H_{2}X_{2}]$ (5)

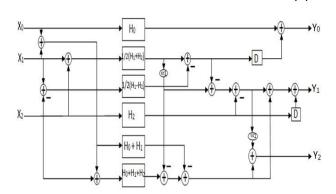


Figure 4: Implementation of the proposed structure 3B

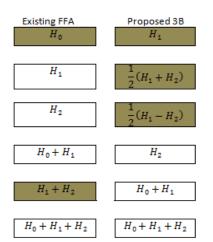


Figure 5: Comparison of Subfilter between Existing FFA and proposed structure 3B

3) Proposed structure 3C with RCA ((N mod 3 = 2)).

In odd length N for a symmetric coefficients, when (N mod 3 = 2), which is presented in (6) can earn one more subfilter block which containing symmetric coefficients as [11],by using ripple carry adder we can reduce the area . The implementation is shown in fig. 6 and the Comparison of Subfilter between Existing FFA and the proposed structure 3C is shown fig.7.

$$Y_{0} = (H_{0} + H_{1})(X_{0} + X_{1}) - \frac{1}{2}[(H_{0} + H_{1})(X_{0} + X_{1}) - (H_{0} - H_{1})(X_{0} - X_{1})] - H_{1}X_{1} + z^{-3} \\ \times \{(H_{0} + H_{1} + H_{2})(X_{0} + X_{1} + X_{2}) - (H_{0} + H_{1})(X_{0} + X_{1}) - [(H_{0} + H_{2})(X_{0} + X_{2}) - \{(H_{0} + H_{1})(X_{0} + X_{1}) - \frac{1}{2}[(H_{0} + H_{1})(X_{0} + X_{1}) - (H_{0} - H_{1})(X_{0} - X_{1})] - H_{1}X_{1}\} \\ Y_{1} = \frac{1}{2}[(H_{0} + H_{1})(X_{0} + X_{1}) - (H_{0} - H_{1})(X_{0} - X_{1})] - H_{1}X_{1}\} \\ Y_{2} = H_{1}X_{1} + [(H_{0} + H_{2})(X_{0} + X_{2}) - [(H_{0} + H_{1})(X_{0} + X_{1}) - (H_{0} - H_{1})(X_{0} - X_{1})] + z^{-3}H_{2}X_{2} \\ Y_{2} = H_{1}X_{1} + [(H_{0} + H_{2})(X_{0} + X_{2}) - [(H_{0} + H_{1})(X_{0} + X_{1}) - \frac{1}{2}[(H_{0} + H_{1})(X_{0} - X_{1})] - H_{1}X_{1}] - H_{1}X_{1} - H_{2}X_{2}]$$
(6)

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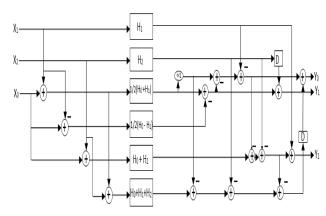


Figure 6: Implementation of the proposed structure 3C

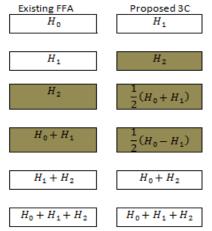


Figure 7: Comparison of Subfilter between Existing FFA and proposed structure 3C

A comparison between the existing FFA and the Proposed FFA is shown in Table 1 below

Table 1: Synthesis	results for	Three j	parallel 27	tap FIR filter
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Structure	CSA(Existing)	CA(Proposed)
3-parallelFIR filter	17184	15124
FIR filter 3A	17133	14799
FIR filter 3B	16055	13794
FIR filter 3C	14841	12942

Simulation Results for comparing the existing and proposed structure is given below

Existing	FIR	filter

FPGA Design Summary	C:/Users/SHOOTER/Desktop/mis/3P_x_27/rajul/rajul.ise -intstyle ise -p xc2s200e-tz356-7 -cm area -pr b -k 4 -c 100 -tx off -o FARALLEL_S_map.nod PARALLEL 3.ndp FARALLEL 3.pcf			
Errors and Warnings	Target Device : x028200e Target Package : ft256			
Synthesis Messages				
Translation Messages	Target Speed : -7			
Map Messages	Mapper Version : spartan2e \$Revision: 1.34 \$			
Place and Route Messages	Mapped Date : Wed Feb 12 11:27:03 2014			
Timing Messages	Design Summary			
All Current Messages	. Number of errors: 0			
Detailed Reports	Number of warnings: 0			
Synthesis Report	Logic Utilization:			
Translation Report	Number of 4 input LUTs: 2,832 out of 4,704 60%			
Map Report	Logic Distribution:			
Place and Route Report	Number of occupied Slices: 1,538 out of 2,352 65%			
Static Timing Report	Number of Slices containing only related logic: 1,538 out of 1,538 100%			
	Number of Slices containing unrelated logic: 0 out of 1,538 0%			
Bitgen Report	*See NOTES below for an explanation of the effects of unrelated logic			
ip Report	Total Number of 4 input LUTs: 2,832 out of 4,704 60%			
Section 1: Errors	Number of bonded IOBs: 144 out of 178 80%			
Section 2: Warnings	IOB Flip Flops: 24			
Section 3: Infos	Number of GCLKs: 1 out of 4 25%			
Section 4: Removed Logic Summary	E Number of GCLKIOBs: 1 out of 4 25%			
Section 5: Removed Logic Section 6: IOB Properties Section 7: RPMs Section 8: Guide Report	Total equivalent gate count for design: 17,184 Additional JTAG gate count for IO8s: 6,960 Peak Memory Usage: 177 MB			

Proposed FIR filter

	xc2s200e-ft256-7 -cm area -pr b -k 4 -c 100 -tx off -o PARALLEL_3_map.ncd
M reasa nepus	PARALLEL 3.ngd PARALLEL 3.pof
Clock Report	Target Device : xc2s200e
S Errors and Warnings	Target Package : ft256
- Synthesis Messages	Target Speed : -7
- Translation Messages	Mapper Version : spartan2e SRevision: 1.34 S
Map Messages	Mapped Date : Wed Feb 12 11:57:21 2014
- Place and Route Messages	Design Summary
- 📝 Timing Messages	
Bitgen Messages	Number of errors: 0
Al Current Messages	Number of warnings: 0
3 Detailed Reports	Logic Utilization:
Synthesis Report	Number of 4 input LUTs: 2,489 out of 4,704 52%
Translation Report	Logic Distribution:
- Map Report	Number of occupied Slices: 1,353 out of 2,352 57%
	Number of Slices containing only related logic: 1,353 out of 1,353 1004
Place and Route Report	Number of Slices containing unrelated logic: 0 out of 1,353 0W
Static Timing Report	*See NOTES below for an explanation of the effects of unrelated logic
🗋 Litgen Repot	Total Number of 4 input LUTs: 2,489 out of 4,704 52%
lao Report	Number of bonded IOBs: 144 out of 178 80%
- Section 1: Errors	IOB Flip Flops: 24
- Section 2: Warnings	Number of GCLHs: 1 out of 4 25%
- Section 3: Infos	Number of GCLKIOBs: 1 out of 4 25%
- Section 4. Removed Logic Summary	
Section 5: Removed Logic	Total equivalent gate count for design: 15,126
- Section 6: 108 Properties	Additional JIAG gate count for IOBs: 6,960
Section 7: RPMs	Peak Memory Usage: 177 MB

FPGA Design Summary	 100 -tx off -o PROF_3A_map.ncd PROF_3A.ngd PROF_3A.pcf Target Device : xc2s200e
Clock Report	Target Package : ft256
Errors and Warnings	Target Speed : -7
Synthesis Messages	Mapper Version : spartan2e SRevision: 1.34 \$
Translation Messages	Mapped Date : Wed Feb 12 11:41:16 2014
Map Messages Place and Route Messages	Design Summary
Timing Messages	Number of errors: 0
D Boon Messages	Number of warnings: 0
Al Current Messages	Logic Utilization:
Detailed Reports	Number of 4 input LUTs: 2,814 out of 4,704 59%
Synthesia Report	Logic Distribution:
Translation Report	Number of occupied Slices: 1,491 out of 2,352 634
Z Map Report	Number of Slices containing only related logic: 1,491 out of 1,491 1009
Place and Poute Report	Number of Slices containing unrelated logic: 0 out of 1,491 04
	*See NOTES below for an explanation of the effects of unrelated logic
Static Timing Report	Total Number of 4 input LUTs: 2,814 out of 4,704 59%
Bitgers Report	Number of bonded IOBs: 144 out of 178 80%
Proof	IOB Flip Flops: 24
Section 1: Errors	Number of GCLKs: 1 out of 4 25%
Section 2: Warnings Section 3: Infos	Number of GCLKIOBs: 1 out of 4 25%
Section 4: Removed Logic Summary 1 Section 5: Removed Logic	Total equivalent gate count for design: 17,133 Additional JTAG gate count for IOBs: 6,960 Peak Memory Usage: 178 MB

Proposed 3A

E FPGA Design Summary	Command Line : C:\Xilinx\bin\nt\map.exe -ise C:/Documents Settings/VLSI/Desktop/ODD LENGTH CODE/PROP 3A/PROP 3A/Pro 3e
Clock Report Servers and Warmings Synthesis Messages Translation Messages Map Messages Map Messages Proce and Route Messages Transp Messages Map Messages Map Messages Map Messages Map Messages Statute Messages	<pre>-intstyle ime -p xc2s200e-ft155-7 -cm area -pr b -k 4 -e 100 PhOD_3A_map.nod PKOP_3A.hpd PKOP_3A.pcf Target Paokage : ft256 Target Paokage : ft256 Target Speed : -7 Mapper Version : spattan2e fRevision: 1.34 f Mapped Date : Thu bec 06 13:31:27 2012 Design Summary</pre>
Map Report Place and Route Report Static Timing Report Report Report	Number of 4 input LUTs: 2,433 out of 4,704 514 Logic Distribution: Number of occupied Slices: 1,319 o Number of Slices containing only related logic: 1,319 o
ap Report Section 1: Encrs Section 2: Warnings Section 3: Infore Section 4: Removed Logic Summary Section 6: IDI Properties Section 7: INFets Section 9: Grade Report Section 9: Grade Report	Number of Slices containing unrelated logic: 0 o *See NOTES below for an explanation of the effects o Total Number of 4 input LUTer: 2,433 out of 4,704 514 Number of bonded 108s: 144 out of 178 804 IOS Flip Flops: 144 out of 178 804 Number of OCLKS: 1 out of 4 254 Number of OCLKS: 1 out of 4 254 Total equivalent gate count for design: 14,709 Additional JTMG gate count for IOBs: 6,600

Existing 3B

T FPGA Design Summary	
M HING WANNAME	Design Information
Priout Report	
Clock Report	Command Line : C:\Xilinx\bin\nt\map.exe -ise C:/Users/SHOOTER/Desktop/mis/PROP
C Errors and Warnings	38-CSA/raju3/raju3.ise -intstyle ise -p xc2s200e-ft256-7 -cm area -pr b -k 4 -c
Synthesis Messages	100 -tx off -o PROP 3B map.nod PROP 3B.ngd PROP 3B.pof
Translation Messages	Target Device : xc2s200e
D Map Messages	Target Package : ft256
Place and Route Messages	Target Speed : -7
Timing Messages	Mapper Version : spartan2e SRevision: 1.34 \$
	Mapped Date : Wed Feb 12 11:46:22 2014
- Etgen Mesnages	
Al Current Messages	Design Summary
C Detailed Reports	
Synthesis Report	Number of errors: 0 Number of vernings: 0
Translation Report	
Map Report	Logic Utilization:
Place and Route Report	Number of 4 input LUTs: 2,659 out of 4,704 56%
Static Timing Report	Logic Distribution:
E outer thing capes	Number of occupied Slices: 1,404 out of 2,352 59% Number of Slices containing only related logic: 1,404 out of 1,404 100%
Map Report	
Section 1: Errors	
Section 2: Warnings	*See NOTES below for an explanation of the effects of unrelated logic Total Number of 4 input LUTs: 2,659 out of 4,704 56%
Section 3: Infos	Number of banded Volter 134 and at 128 746
Section 4: Removed Logic Summary	I wamper of pounded topp: 126 onc of 110 lee
Section 5: Removed Logic	Total equivalent gate count for design: 16,005
Section 6: 108 Properties	Additional JTAS gate count for IOBs: 6,528
Section 7: RPMs	Peak Memory Usage: 177 MB
Section 8: Guide Report	reak heady usage: 1// np

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Proposed 3B

	I Toposed 5D
Timing Messages User Messages At Current Messages At Current Messages Seleved Reports Seleved Report Place and Route Report Static Timing Report Stops	Design Summary
Report Section 1: Errors Section 2: Warrings Section 3: Infore Section 4: Removed Logic Section 6: Removed Logic Section 6: IOB Poporties Section 7: RPMs Section 8: Guide Report Section 8: Guide Report Section 8: Guide Report	*See NOTES below for an explanation of the effects of Total Number of 4 input LUTs: 2,267 out of 13,824 16% Number of bonded IOBs: 136 out of 325 41% Number of OCLXs: 1 out of 4 25% Number of GCLXIOSs: 1 out of 4 25% Total equivalent gate count for design: 13,794 Additional JTAG gate count for IOBs: 6,576 Peak Memory Usage: 146 MB

Existing 3C

TFPGA Design Summary +	Release 8.11 Map I.24
M liming Constraints	Xilinx Mapping Report File for Design 'PROP_3C'
Prout Report	
Oock Report	Design Information
BErrors and Warnings	
Synthesis Messages	Command Line : C:\Xilinx\bin\nt\map.exe -ise C:/Users/SHOOTER/Desktop/mis/PROB
Translation Messages	3C-C3A/raju4/raju4.ise -intstyle ise -p xc2s200e-ft256-7 -cm area -pr b -k 4 -c
Nap Messages	100 -tx off -c PROF_3C_map.ned PROF_3C.ngd PROF_3C.pcf Target Device : xc2s200e
Race and Route Messages	Target Package : ft256
Timing Messages =	Target Speed : -7
Elitern Messages	Mapper Version : spartan2e \$Revision: 1.34 \$
Al Current Messages	Mapped Date : Wed Feb 12 11:51:02 2014
B Detailed Reports	
	Design Summary
Synthesis Report	
Translation Report	Number of errors: 0
Map Report	Number of warnings: 0
Place and Route Report	Logic Utilization:
Static Timing Report	Number of 4 input LUTs: 2,465 out of 4,704 52%
lap Report +	Logic Distribution:
Section 1 Errors	Number of occupied Slices: 1,304 out of 2,352 55% Number of Slices containing only related logic: 1,304 out of 1,304 100%
Section 2: Warnings	Number of Slices containing only related logic: 1,304 out of 1,304 100% Number of Slices containing unrelated logic: 0 out of 1,304 0%
- Section 3: Infos	"See NOTES below for an explanation of the effects of unrelated logic
Section 4: Renoved Logic Summary E	Total Number of 4 input LUTs: 2,465 out of 4,704 52%
- Section 5: Removed Logic - Section 6: IOB Properties	Number of bonded IOBs: 128 out of 178 714
Section 7: RPMs	
- Section 8: Guide Report	Total equivalent gate count for design: 14,841
- Section 9 Jack Crown Comman	Additional JTAG gate count for IOBs: 6,144

Proposed 3C

Al Current Messages Detailed Reports Synthesis Report Translation Report	Design Summary Number of errors: 0 Number of warnings: 0 Logic Utilization:
Map Report	Number of Slice Flip Flops: 24 out of 13,824 14
Place and Route Report Static Timing Report	Number of 4 input LUTs: 2,124 out of 13,824 154 Logic Distribution:
Bilgen Report	Number of occupied Slices: 1,147 ou
p Report Section 1: Errors Section 2: Warnings	 Number of Slices containing only related logic: 1,147 ou Number of Slices containing unrelated logic: 0 ou *See NOTES below for an explanation of the effects of
Section 3 Infor	Total Number of 4 input LUTs: 2,124 out of 13,824 15%
Section 4: Removed Logic Summary	Number of bonded IOBs: 128 out of 510 25% Number of GCLKs: 1 out of 4 25%
Section 5: Removed Logic Section 6: IOB Properties	Number of GCLKIOBs: 1 out of 4 25%
Section 7: RPMs Section 8: Guide Report Section 9: Area Group Summary	Total equivalent gate count for design: 12,942 Additional JTAG gate count for IOBs: 6,192 Peak Memory Usage: 146 MB

4. Conclusion

In this paper we have brief, we have presented the parallel FIR structure which is reduced the area. Multipliers are major component which we can be replaced by using the fast FIR algorithm. In this paper we presented ripple carry adder in the odd length instead of carry save adder.

5. Future Scope

The future scope of this project lies in the further optimization of area and as well as power.

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Author Profile

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