Design and Implementation of Ternary Bidirectional Barrel Shifter Using Multi-Valued Reversible Logic

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Abstract: *Reversible logics are a promising application for low power computing, quantum computing and other emerging computing technologies. The application of multi-valued logic reduces the width of reversible and quantum computing gates. Barrel shifters are being used for high speed data shifting. In this paper, we propose a ternary bidirectional barrel shifter design which is a combination of Ternary Feynman and Modified Fredkin Gate. The proposed design is evaluated in terms of Operations, Garbage outputs, Quantum cost and the number of Ancilla inputs.*

Keywords: Quantum cost, Ancilla inputs, Garbage output, Modified Fredkin gate, Ternary Feynman gate.

1. Introduction

In most kinds of mathematical operations that been done in digital world needs shifting and rotation operations. Some of those applications are convolution, correlation, multiplication, etc. This demand made the use of shifters as important functional part in modern computers. To make these shifters faster in response the barrel shifters are being proposed. Barrels shifters can shift data in one single clock cycle and they don't have an inbuilt memory this makes the systems to be in faster response when compared with other flip flop shifters.

Low power systems had become an important factor since transistor sizing was being drastically been reduced, as the size of transistors were reduced as per Moore's law, their corresponding heat generation also came up this means that loss of information's. This was an unacceptable part. To reduce this loss of information, reversible logics are being proposed. Here in reversible logics one to one mapping is being used between input and output vectors. Thus, one to one mapping is proven to reduce the power dissipation than when compared with other conventional logic gates.

In conventional logics one output was being followed from many fan-in's, this creates a loss of power as in the form of heat. This loss of heat is considered as loss of information. According to Laundauer [1], if a system is irreversible then a bit of erasing can cause a *KTln2* Joules of energy, where K is the Boltzmann's constant and T is the absolute temperature of the environment. This *KTln2* joules of heat dissipation of heat can be avoided if the computation is done reversible logic design [2]. Reversible logic got a wide application in quantum computing, optical computing etc.

The major application of reversible logic comes under quantum computing, where in quantum computing they perform several unitary operations such as if we consider a conventional logic the states of the operation is 0 and 1, but when it comes under quantum logic, the operations are 0, 1 and superposition of 1 and 0. These operands are called qubits. Where Qubits are said as quantum preliminary operations. And cost of performance of each gate is considered under the quantum cost of every individual gate.

2. Basic Reversible Gates

In reversible logics, the gates must have a 'n inputs and n outputs'. Where in ideal case it's considered as these NxN logic structures will not dissipate *KTln2* heat and there won't be any power dissipations, but when practical case is considered the reversible gates produce *KTln1* amount of heat to the atmosphere. Thus the amount of power dissipation and information loss is reduced [3]. There are several basic gates such as Toffoli gate, Feynman gate, Peres gate, TR gate, etc. [8], [9], [10].

When reversible logics are compared among conventional logic diagram, there are several unwanted outputs or several unused outputs, these outputs are said as Garbage outputs. And some of constant inputs are being given to reversible logics to produce desired output character to reversible logic gates, these inputs are called as Ancilla inputs. The quantum cost of reversible gates is equal to the number of 1x1,2x2 and 3x3 reversible gates that been used for the design. The quantum cost of 1x1 and 2x2 are considered as unity [12], [13].

2.1 The NOT GATE

1X1 gate is NOT gate represented in fig 1 performs the equal operation to conventional not gate which gives negation to input.
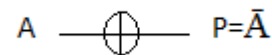
Figure 1: NOT GATE

2.2 Controlled –V and V+ Gates

In a control –V gate, there is one control signal which controls the other input signal. When A=0 then the qubit will be bypassed unchanged. When A=1 then unitary operations are performed $V = \frac{i+1}{2}\begin{pmatrix} 1 & -i \\ -i & 1 \end{pmatrix}$ is applied to B input.
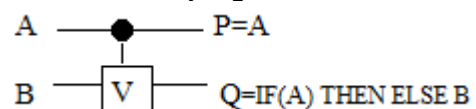
Figure 2: Controlled V Gate

2.3 Feynmam Gate

Feynman gate is 2x2 gate, as in the fig. 3 .The Feynman gates are being used for fan-out operations or to get complement of the input, here input B act as a control signal and where if input B is 0 then at output A is being achieved at both output ports else, when if B=1 the one output port gives A and the other gives $\bar{A}$, thus mostly Feynman gates are used for fan –out operation. The quantum cost of feynamn gate is one [4].
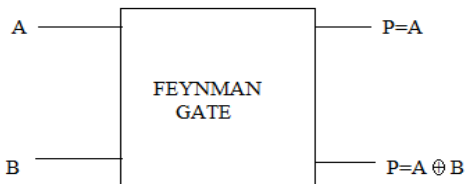

Figure 3: Feynman gate

2.4 Fredkin gate

The Fredkin gate is 3x3 gate where its quantum cost is 5. The fredkin gate is composed of a control signal A and two other inputs B and C where it act as a multiplexer and the control signal act as select line. The output also is three port P,Q and R ,where one is the control signal itself P and the other are swapped or sent as of input according to the control signal , where of the control signal A =0. Then Q=B and R=C else if A=1 then Q=C and R=B [14].
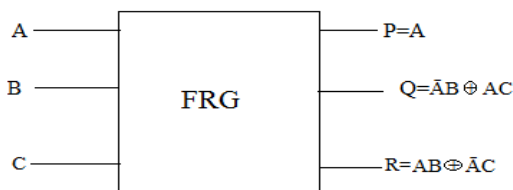

Figure 4: Fredkin Gate

3. Ternary Reversible Gates

The major application of reversible logic gates comes under quantum computing. As per conventional logics are concerned, it has two operational states such 0 and 1, while when qubits are composed just more than more than two states, as super imposition of 0 and 1, These states are called multi-valued logic states. Multi valued logics are used to reduce the width of reversible or quantum circuits. Among these multi valued quantum logic, the most widely used are, ternary or trivalent quantum logic [5], [6]. The two conditional input logic gates called Muthukrishnan and Stroud gate (M-S gate).

The M-S gate is physically realizable with ion trap technology. Which was used to implement ternary reversible gates. Ternary reversible gates are composed of three states which are $|0\rangle$, $|1\rangle$ and $|2\rangle$. These gates have a unique mapping between input and output, which can be used in the implementation of ternary modified fredkin gate [5]. In out proposed system we used the modified fredkin gate and ternary feyman gate for the implementation of bidirectional barrel shifter. These ternary reversible gates can be implemented using M-S gates. Where the proposed systems perform several operations like arithmetic and logical left or

right shift and rotate left and write operations. We can suggest that the quantum cost of a ternary reversible logic gates is the number of Muthukrishnan –Stroud gates and shift gates that been used in the design implementation [5].

3.1Ternary Feynman Gate

A ternary reversible gate is 2x2 gate where the output mapping for input are (A, B) to (P=A, Q=A+B), [5] where A is the control signal and its directly out passed through P, and Q is given a sum of A+B. When considering Q, if B=0 the copy of A will be given as output, so ternary Feynman gate can be used to produce copies of input at the same in time to avoid fan out problems. Fig 5 shows the implementation of ternary Feynman gate when realized in M-S gates. The quantum cost of ternary Feynman gate is 4.
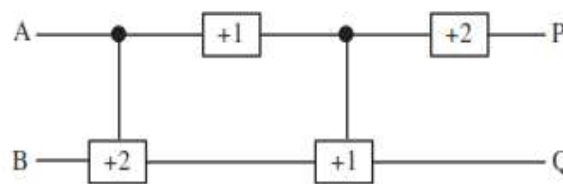

Figure 5: Ternary Feynman gate realized in M-S gates.

3.2 Modified Fredkin Gate

Modified fredkin gate MFG is composed of 4x4 input output mapping where two of those inputs are control signal [5]. MFG is multi valued logic, where the input ports are A, B, C, D and the output ports are P=A, Q=B, R=C if A<B else D, S=D if A<B else C as shown in fig. 5. In ternary modified fredkin gate A and B are bypassed and also act as a control signal for other two inputs.
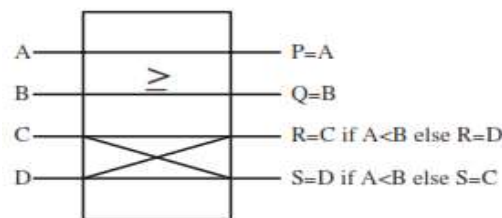

Figure 6: Ternary Modified Fredkin Gate

Modified fredkin gate act as a multiplexer which being used in our proposed design of barrel shifter. The quantum cost of MFG is 41.

4. Barrel Shifter

Barrels shifter in digital circuits is able to shift the data in one single clock cycle, which contains 'n' inputs and 'n' outputs with K control signal to shift the data. These shifters are being designed unidirectional, bidirectional in [5], [11]. Where those designs are being proposed in the logarithmic shifter as shown in fig 7. Among these existing designs, the logarithmic shifters are used such as to reduce the area and to make the design simple by reducing the number of decoders used in the design. There are several existing designs that could perform operations as rotate left, rotate right, shift arithmetic left, shift arithmetic right, shift logic left and shift logic right.

Thus, when we consider more in application of reversible logic, we need to look over the chances of multi valued logic. As in quantum logic the superposition of 0 and 1 leaves multiple values for the operational input as in [15]. The existing patterns are complex and involve heavy number reversible gates. Therefore, by using ternary reversible logic, it cuts down the width of reversible or quantum circuits and at the same time its multi-valued too. The purported purpose of the barrel shifter composed of ternary states of operation.
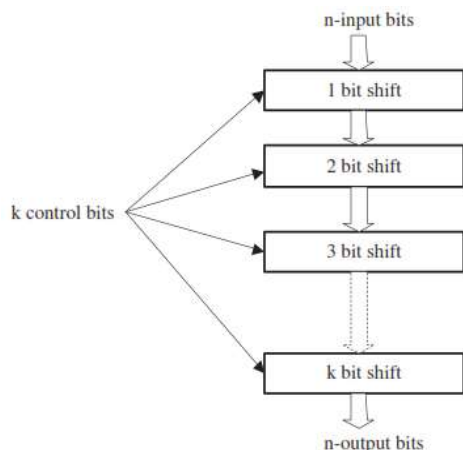

Figure 7: Structure of n, k barrel shifter

5. Proposed Reversible Bidirectional Barrel Shifter

The proposed design is composed of several operations such as it can perform logic left & logic right shift, arithmetic left and right shift, rotate left and rotate right operations. These operations are controlled by several control signals such as s0, s1, s2, sra, sla, rot and left. Where s0 ,s1, s2 are control signals that used to shift the input data and see for shift right accumulator , sla to shift left accumulator , left to shift logic left and when left is '0' it shifts right, 'rot' to rotate input data in a cyclic manner. The pattern of these control inputs are being explained in table 1.

The design can be explained in six modules, along with their control signals as (i) Data reversal control unit- I 'left', (ii) Arithmetic right shift control unit 'sra', (iii) Rotation unit 'rot', (iv) Shift control unit as stage1 's2', stage2 's1', stage3 's0', (v) Arithmetic left shift control unit 'sla', (vi) Data reversal control unit-II.

In the proposed design, there are 8 input ports and three shift control units. These control units are used to control the number of shifts that to be performed. Where in arithmetic right shifts the control unit sra, preserves the sign digit and at arithmetic left shift sla, it generates '0'. Different the shift operations are being explained in table II, and the proposed design is plotted in the fig. 8.
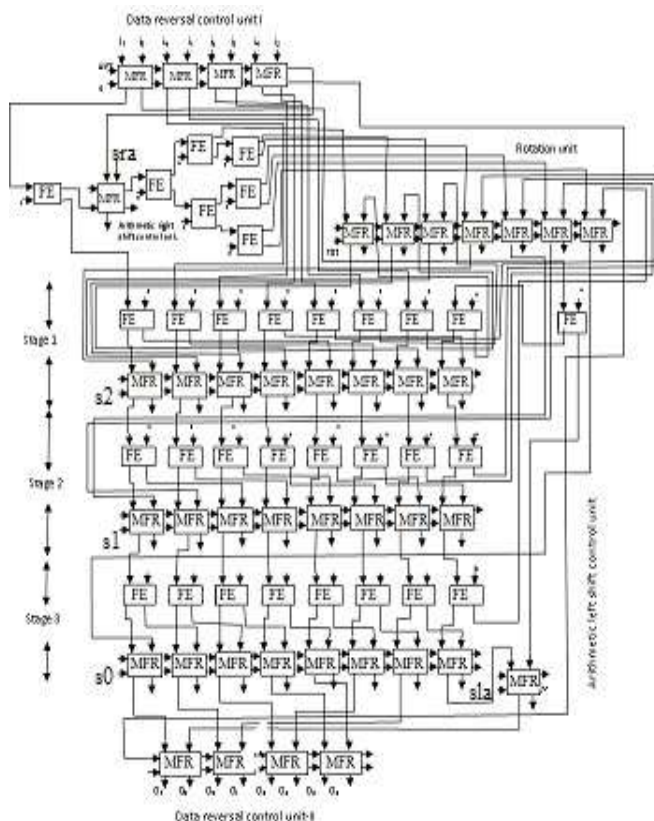

Figure 8: Proposed Ternary bidirectional barrels shifter *FE represents Modified Feynman gate and MFR represents Modified Fredkin gate

Table 1: Input Control Signal to Perform Shift Operation

Shift	Control signal inputs			
Logical	Left=0	Rot=0	Sra=0	Sla=0
Arithmetic	Left=0	Rot=0	Sra=1	Sla=0
Rotate right	Left=0	Rot=1	Sra=0	Sla=0
Logical left	Left=1	Rot=	Sra=0	Sla=0
Arithmetic	Left=1	Rot=0	Sra=0	Sla=1
Rotate left	Left=1	Rot=1	Sra=0	Sla=0

Table 2: Operations Performed by when, K=3 in Bi - directional Barrel shifter

Operations	Y
shift right logical	000i7i6i5i4i3
shift right arithmetic	i7i7i7i7i6i5i4i3
rotate right	i2i1i0i7i6i5i4i3
shift left logical	i4i3i2i1i0000
shift left arithmetic	i7i3i2i1i0000
rotate left	i4i3i2i1i0i7i6i5

6. Performance Evaluation

The (8, 3) ternary bidirectional barrels shifter using multi value reversible logic that's been explained in the fig 8, uses modified to solve fan-out issue and modified fredkin gate to act an 2:1 multiplexer these gates perform shifting operation in logarithmic basis as each stage performs a particular shifting as stage 1 performs forced four bit right shifting, stage 2 performs two bits right shifts and stage 3 performs one but right shift. In the proposed design it's been designed with Feynman gate is have 41modified fredkin gate (MFR) and 32 feynman gate, which performs barrels shifter operations. In ternary gates the design is being done with M-S gates and shift gates where the summation of these two gates gives quantum cost of the design.

6.1 Ancilla input bits

Ancilla inputs are constant inputs to the reversible gates. In reversible gates fan-out operations are not allowed, thus Feynman gates are being used. Thus to make copies of the port 'A' we give a constant input '0' to port 'B' in fig 5. This gives a copy of port 'A' in two outputs 'P' and 'Q'. (n,k) reversible bi-directional shifter fan-out operation. Table III shows the number of ancilla inputs used to different (n,k) barrel shifter.

Table 3: Pncilla Input (n,k) Ternary Reversible Bidirectional Barrel Shifter

n/k	n=4	n=8	n=16	n=32	n=64
K=2	13	21	37	69	133
K=3		33	57	105	201
K=4			81	145	273
K=5				193	353
K=6					449

6.2 Quantum cost

The quantum cost is the number of quantum preliminary operations that been performed in a reverse gate. The reversible Feynman gate have a quantum cost '1' and fredkin gate have a quantum cost '5'. And Modified Fredkin Gate have a quantum cost of 41 and Modified Feynam Gate is 4. While considering our proposed design the *Quantum Cost = 41*(number of modified fredkin gates) + 4*(number of modified feynam gates).* Thus the quantum cost of the proposed systems can be up to 1809.

6.3 Garbage outputs

Garbage outputs are the un-used outputs of reversible logic gates ,where its considered as the waste of energy During analysis its observed that (n,k) barrels shifters the garbage outputs are directly depending on to the value of n and k. In ternary reversible logics the garbage output is comparatively higher than that of previous papers. These unwanted outputs occurs due to the ternary states which are being unused in the barrel structure design. In the proposed design the garbage output was 39.

7. Implementation and Result

The proposed design was functionally verified and results are verified. The transistor cost was observed in analog flow. The functional design was verified in Xilinx. The output waveform of 3 bit arithmetic shift is shown in fig 9.
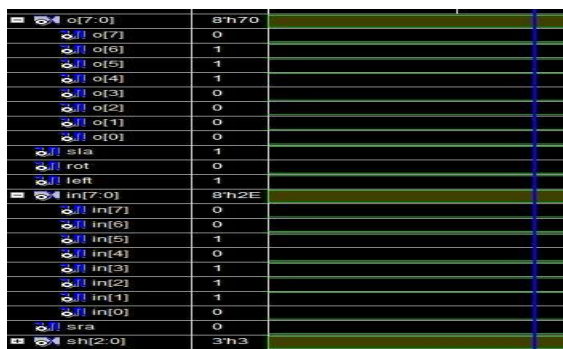

Figure 9: An 8 bit arithmetic left shift simulation output waveform.

8. Conclusion

In this paper a novel architecture of ternary bidirectional barrel shifter using multi valued reversible logics are proposed. The proposed design used ternary reversible gates, which were an application of M-S gates. The design was evaluated in terms of quantum cost, ancilla inputs and garbage output. The functional verification of the proposed design was done using verilog HDL and observed that the ancilla inputs and the quantum cost vary rapidly with the n and k value variation. The functional verification of the proposed design is done in Xilinx ISE14.1i. The proposed ternary bidirectional barrels shifter got a wide application digital signal processing systems.

9. Future Enhancement

The enhancement of this paper can be done in optimization of garbage output and reduction in quantum cost. Thus the power consumption can be reduced to a greater extend and an effective low power design can be obtained.

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