Design of Low Power Novel Viterbi Decoder Using Multiple Threshold CMOS Logic

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Abstract: ***In this paper a low power viterbi decoder based on multiple threshold CMOS logic is presented. In wireless communication, viterbi decoder which consumes more power plays an important role. viterbi decoder is used to decode the received data which is encoded using convolution codes. In this paper in order to reduce the power consumption and to improve the performance of the decoder optimized gate logic is proposed. As the multiplexer and flip- flops are the major parts in the viterbi decoder circuit, multiple threshold CMOS (MTCMOS) logic is used to reduce the complexity of the circuit. The proposed technique is simulated using tanner tool. The simulated result shows the power consumption of viterbi decoder using MTCMOS is lower compared to CMOS logic and also the number of transistors required to design the viterbi decoder is reduced using MTCMOS logic.***

Keywords: Viterbi decoder, multiple thresholds, tanner tool

1. Introduction

Viterbi decoder [1] is based on viterbi algorithm which was proposed by Viterbi in 1967.The algorithm is mainly used to decode the convolution codes in digital communication systems. The viterbi algorithm (VA) provides the most accurate way to find maximum likelihood sequence of transmitted signal. In order to transmit the analog signal through the digital communication system, the signal should be sampled and quantized before proceeding through the system. In this paper, it is assumed that the digital values are transmitted through channel. The viterbi algorithm is used to find the signals which are corrupted by noise in the channel.

The viterbi decoder consists of three major blocks such as branch metric unit, add compare and select unit and survivor memory unit. The Viterbi algorithm is based on treills diagram and the encoder circuit is considered as a finite state machine. In order to find out the errors in the received sequence the hamming distance of that sequence is calculated.

Viterbi decoders are widely used in wireless communication specifically in third generation mobile terminals and it consumes more power in the transmission system. In present scenario reducing the power consumed by a device is a major factor in VLSI technology. Even though the CMOS logic design plays a major role in designing devices with low power consumption, the switching activity of the CMOS devices causes more power consumption. For low power consumption, different logic styles may be used to minimize the power consumption. In this paper, the design based on multiple threshold CMOS logic is proposed for low power consumption application.

2. Proposed Design

The proposed method is based on multiple threshold CMOS logic (MTCMOS). The general structure of MTCMOS is shown in figure 1.The MTCMOS is one of the low power techniques which reduce the leakage power. In this logic, the different threshold voltages are selected by varying length and width ratio of the channel in both nMOS and pMOS transistors.The high Vt transistors are used in non critical path of the logic and low Vt transistors are used in critical path of the logic.The sleep transistors with high Vt form the virtual power supply and ground in order to reduce the power during standby mode.

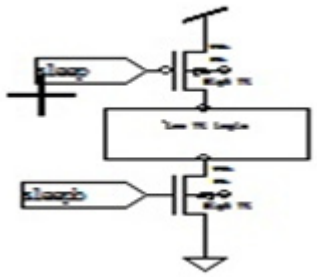

Figure 1: Structure of MTCMOS Logic

3. Design of viterbi decoder using MTCMOS

The Viterbi decoder consists of three major blocks such as Branch metric unit, Add compare and select unit and Survivor memory unit. In this chapter the blocks of viterbi decoder are explained using multiple threshold CMOS logic.

3.1 Branch Metric Unit

The Branch Metric Unit (BMU) is used to measure the Hamming Distance between the received sequences with the

expected code sequence. The Hamming Distance is calculated simply by counting the number of bits at which the received sequence and the expected sequence are different. The BMU consists of a two input EXOR gate and three bit asynchronous counter. The counter is designed using T flip-flops. The output of the EXOR gate is applied as the clock pulse to the first flip flop of the counter and output of one flip-flop is given as clock input for the next flip flop. The T input for all flip-flops are tied to HIGH input. When the received sequence and the expected sequence are different then the output of the EXOR gate becomes high and the counter starts to count. The circuit diagram for BMU is given in the figure2.The counter is designed by cascading T flip-flops and the T flip-flop is designed by using D flip-flop and gates. The circuit diagram for D flip-flop using MTCMOS is shown in figure 3.

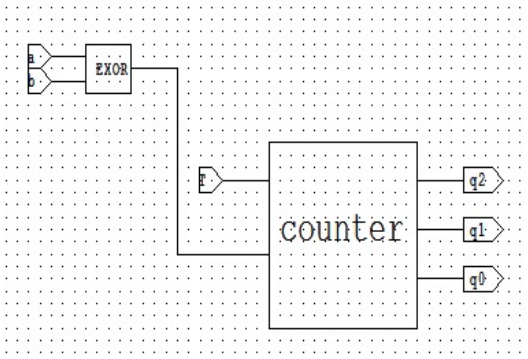

Figure 2: Block Diagram of BMU

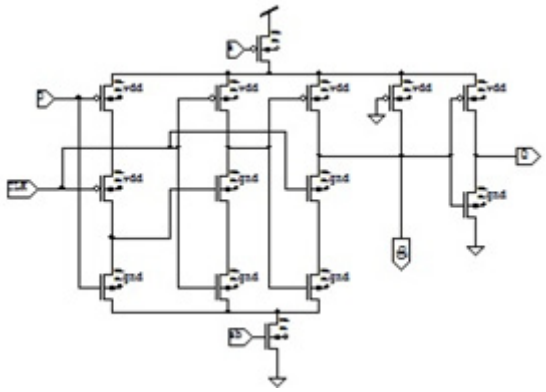

Figure 3: Circuit Diagram for D FF using MTCMOS

3.2 Add Compare and Select Unit

The Add Compare and Select unit (ACSU) consists of adder, comparator and selector. The adder unit adds the branch metric from the BMU with the corresponding path metric. The inputs to the adder are the output of BMU and the previous path metrics.

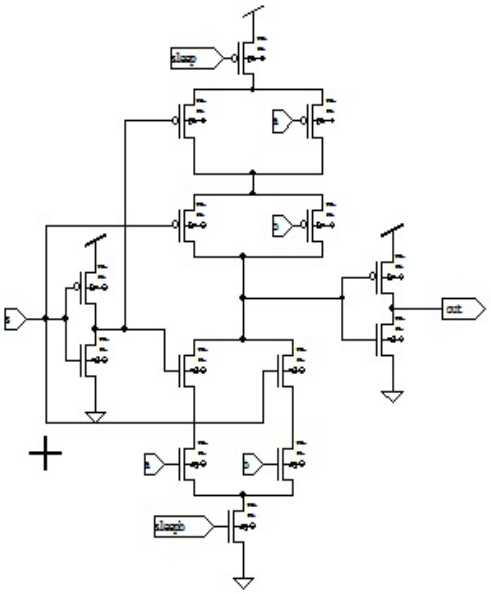

Figure 4: Circuit diagram for 2 to 1 multiplexer using MTCMOS

The new resultant metrics are compared in comparator. The multiplexer is the major block in the selector. The circuit diagram for multiplexer using MTCMOS is shown in figure4.The selector selects the appropriate branch. The selector unit consists of four 2:1 multiplexers. The outputs of adder unit are given as inputs to the selector unit. The output (less than bit) of the comparator is given as selection line for the selector.

3.3 Survivor Memory Unit

The important step in the decoding process is finding the survivor path. The output of the selector is the survivor path and that path is stored in the survivor memory unit. The survivor memory unit (SMU) is designed by cascading serial in serial out (SISO) shift registers. The length of the shift registers depends on the length of the encoder. The SMU unit consists of four SISO shift registers. When the positive clock pulse is applied, the data D is transferred to the output of the flip-flop and for each positive clock cycle the value stored in one register is shifted to another register.

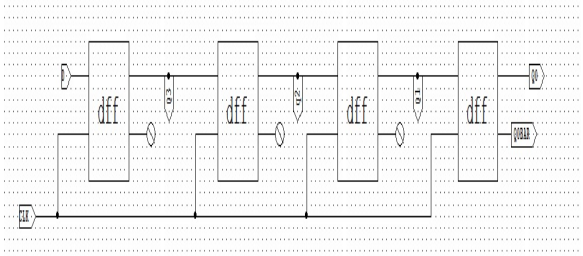

Figure 5: Block diagram of single stage of SMU

3.4 Block diagram of viterbi Decoder

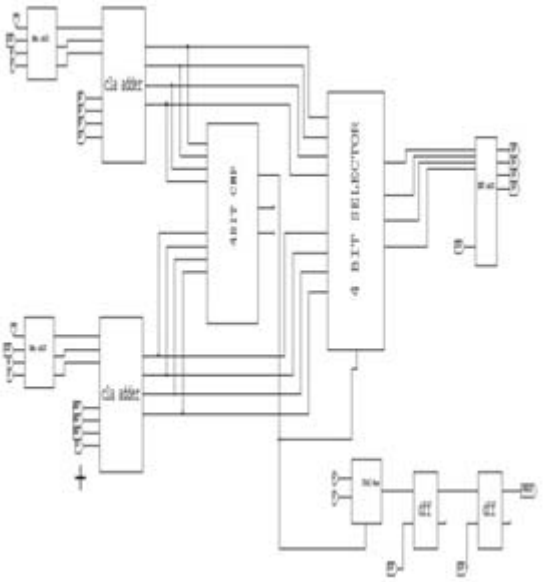

Figure 6: Block diagram of viterbi decoder

The block diagram of viterbi decoder with MTCMOS is shown in figure 6.The circuit is designed using Tanner tool. In this circuit two BMU units are used since there are two possible state changes from one state to another state. The BMU unit calculates the branch metric. The ACSU adds the branch metric with the previous path metric using adder. The comparator adds two paths from two adders and the selector selects the path with minimum hamming distance .The SMU stores the new path metric value and the corresponding states. The 2:1multiplexer and two bit shift registers are used to get the decoded output.

4. Results and Discussion

The viterbi decoder designed using MTCMOS logic are simulated using Tanner tool (TSPICE) in 20µm technology. The output waveform of the viterbi decoder is shown in the figure7.When the select input is logic 1, then the 'a' input value is transferred to the output. In the BMU the clock signal for the counter is applied from the output of EXOR gate. There are two BMUs since each state has two branches in treills.

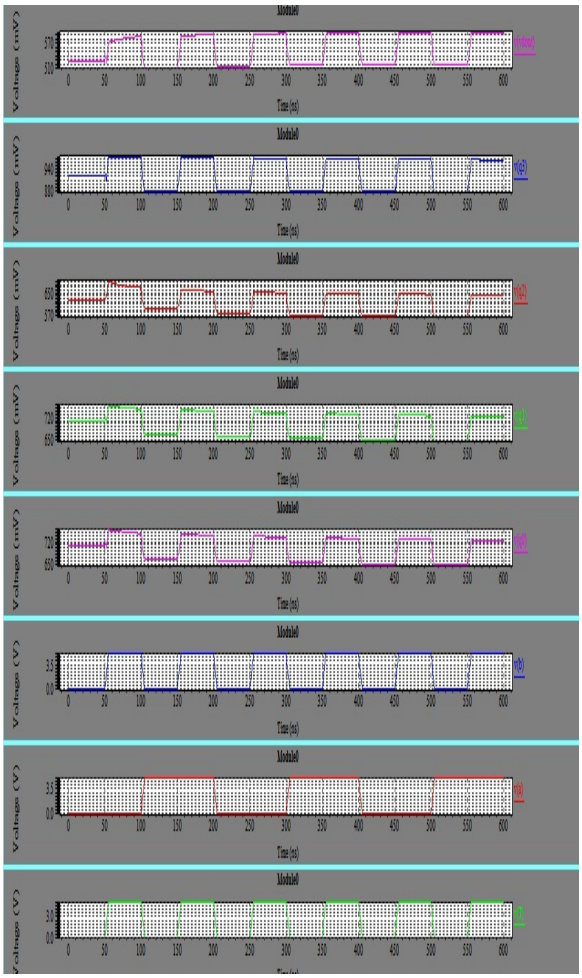

Figure 7: Output waveform of Viterbi Decoder Using MTCMOS

The output of the EXOR gate is the Hamming distance between the expected sequence and the received sequence that can be counted by using the counter. The output of the BMU denotes the branch metric value. In ACSU the branch metric values are added with the Path metric value and the appropriate path is selected in selector unit using the control signal from the comparator unit. The Less than (LT) output of the comparator is used as a selection line of the selector unit and the multiplexor. When the select input is logic '0', then the 'b' input value is transferred to the output.

4.1 Comparison of Performance

The Viterbi decoder is designed using MTCMOS in circuit level. The performance of viterbi decoder is analyzed using the simulated output in Tanner tool. The simulation results show that the power consumption, the number of transistors of the Viterbi decoder using MTCMOS are reduced while compared to the existing CMOS, Pass transistor logic and Transmission gate logic. Hence the result proves that the proposed

MTCMOS logic has low power, high speed and low area compared to other logics. The performance comparison table for Viterbi decoder with 5v vdd is given in Table1. The performance comparison table for Viterbi decoder with 3v vdd is given in Table2. The performance comparison table for Viterbi decoder with 1.5v vdd is given in Table3.

5. Conclusion

The major blocks of Viterbi decoder are simulated by using Tanner's s-edit VLSI CAD tools and parameters such as power, delay and area are analyzed by using same tool. The circuits were compared with existing circuits. The circuit based on MTCMOS gives better performance than existing circuits in term of power dissipation and area. The proposed circuits can be used in the low power wireless communication systems.

Table 1: Viterbi Decoder with Vdd = 5.0Volts

S. No	*Viterbi Decoder*	*Power (mW)*	*Transistor count*	*Area μm^2*	*Speed (Ghz)*	*Delay (ns)*	*PDP(10^{-12} W-s)*
1	CMOS	628	1114	0.049016	4.276	233.86	146.86
2	PTL	269	584	0.025696	9.042	110.59	29.74
2	TG	355	854	0.036872	13.33	74.98	3.074
4	MTCMOS	26.7	724	0.031856	18.64	53.64	1.432

Table 2: Viterbi Decoder with Vdd = 3.0Volts

S. No	*Viterbi Decoder*	*Power (mW)*	*Transistor count*	*Area μm^2*	*Speed (Ghz)*	*Delay (ns)*	*PDP(10^{-12} W-s)*
1	CMOS	124	1114	0.049016	6.456	154.6	19170.4
	PTL	43.44	584	0.025696	12.47	80.17	3482.58
2	TG	11.24	854	0.037576	14.45	69.32	779.15
4	MTCMOS	7.65	724	0.031856	21.46	46.58	356.33

Table 3: Viterbi Decoder with Vdd = 1.5 Volts

S. No	*Viterbi Decoder*	*Power (mW)*	*Transistor count*	*Area μm^2*	*Speed (Ghz)*	*Delay (ns)*	*PDP(10^{-12} W-s)*
1	CMOS	6.981	1114	0.049016	8.89	112.45	785.01
2	PTL	5.372	584	0.025696	13.43	74.46	399.99
2	TG	4.32	854	0.037576	11.44	87.39	377.52
4	MTCMOS	0.709	724	0.031856	32.36	30.90	21.908

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