This could be coupling and does not carry any dead zone of operation and this could be switching to the prominent to the all stages. The capacitance from the c1 of each branch carries the unit supply of the voltage from clk to clkb. Then the last stage from the n-MOS N1 and this could be coupling with the N2 and then the P1 coupling with the P2 having the amplitude switching. Then this storage from the each stages of the coupling from the node of operation can also to be calculated from the structural of the node 1 to 8. Then another node of bulk connection has been applied from the N1 to the P1 of linear stages. This could be effectively reduces the parasitic capacitance from the charge pump.

This proposed charge pump has advantages of the low power consumption based on body biasing bulk connection from the each node of operation. And also this charge pump circuit has been enabled for the lower input voltage (in milli volts) having the bulk output voltages from the clock pulses. The enabling signals that carry the circuit level of operation from the amplitude degradation of the unit supply to the needed positive up gradation from the input amplitude. This phase difference from the clock pulses into the bulk connection from the unit supply that can be varied as per the input signal.

The required connection between these signals has been proposed and implemented into the phase locked loop. This could be having the phase detector, Charge pump and the voltage controlled oscillator. The level of connection is to be a feedback signal from the VCO to the input voltage. The phase difference from the input and the feedback signals has been applied to the phase detector. Then the charge pump gives the amplification of the input voltage from the phase detector. The variations of the phase frequency has been identified and also applied for the frequency synthesizer.

The combination of the input voltage and the clock pulses that could be given into the application of the phase locked loop, modulators, servo mechanism and the digital communications. The variation cannot be finding from the amplitude and the frequency ranges of the input and the output from 50Hz to 1000MHz. These levels of frequency variation are used for the performance of the amplitude synthesizer.

A feedback charge pump circuit that uses cross-coupled NMOS switches area unit accustomed wins a high boost magnitude relation for a low-tension DRAM word-line driver. This circuit uses 2 capacitors that area unit switched in such the way that in each clock cycle, one electrical condenser is charged to the provision voltage and also the different electrical condenser is boosted to doubly the provision voltage by the clock. The two capacitors reverse roles each clock cycle, inflicting the voltage at the output to be a sq. wave that switches between VDD and 2VDD. 2 of those cross-coupled NMOS pairs area unit used on with Associate in nursing other form of charge pump and an electrical converter to form up the entire boosted voltage generator.

In, the cross-coupled NMOS charge pump introduced and that is employed to boost the speed of pipeline A/D convertor by boosting the clock drive so as to cut back the on-resistance of transmission gates within the pipeline. This work additionally utilizes a bias voltage generator to bias the n-well to double the availability voltage, preventing latch up from occurring throughout the initial startup transient. This architecture has been combined and gives the variations from the each circuit combination to the charge pump coupling into the inverter stages. That could be recognized as per the net list generation of the designing technique from the each coupling of the n-MOS and the p-MOS to the biasing node of operation units in the circuit implementation of the charge pump circuit.

4. Simulation Results

The existing Dickson charge pump circuit and the waveform (Fig 4 &5) are shown. The designing of this charge pump are designed in TANNER EDA.

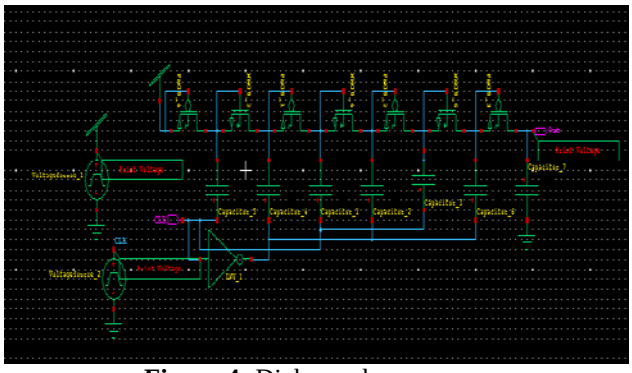

Figure 4: Dickson charge pump

The schematic diagram of proposed charge pump and the resultant output waveform is shown in the figure 6&7.

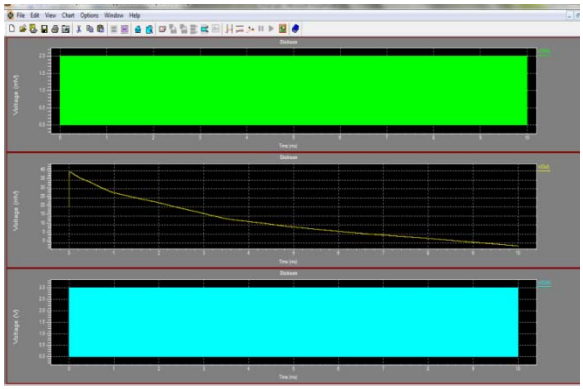

Figure 5: Waveform of Dickson charge pump

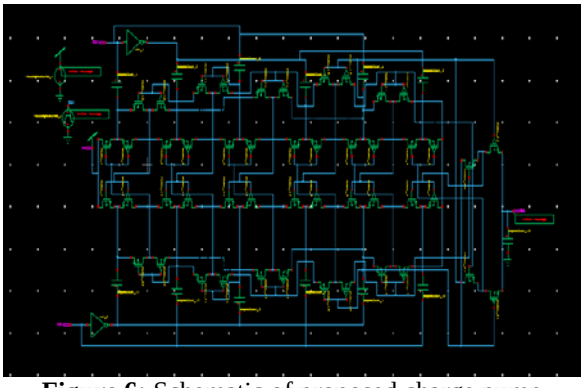

Figure 6: Schematic of proposed charge pump

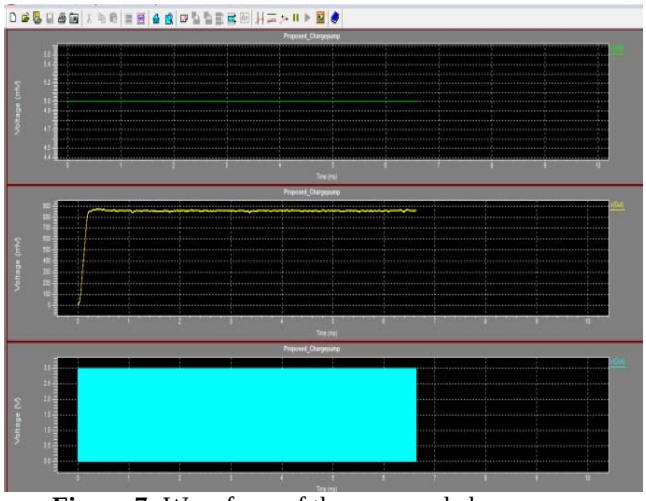

Figure 7: Waveform of the proposed charge pump

The output results of the parameter of power output voltage and the nanometer technology has been illustrated in the table-1. The consideration of this parameter has been verified and then processing of this bulk connection could be established as per the input voltage supply.

Table 1: Parameter results of the charge pump

Charge pump	*Power in watts*	*Output voltage*	*Pumping Efficiency*
Dickson charge pump	8.60 W	50 mV	56%
Wu Chang charge pump	8.04 W	20mV	42%
Linear charge pump	5.84 W	100mV	71%
Proposed charge pump	3.29 W	1000mV	83%

The results has been analyzed and verified by the parameter of the existing and the proposed charge pump. And also the capacitance of these charge pumps has been 1 pF. Then the technology of the nano meter could be used as TSMC CMOS. The operation input voltage is to be in 2mV. The variation of the output amplitude voltage could be obtained from this charge pump of the clock signal to be applied to the input source. The further variation process handled for the low area chip fabrication and for the low power consumption of this proposed charge pump circuit.

5. Conclusion

Charge pump based on body biasing and the backward control scheme has been proposed in this system. The power and the amplification could be efficient when compared to the other existing charge pump. The low output ripple and high system stability of the dual-phase charge pump circuit are demonstrated by the test chip and get better performance. Therefore, the transient response and driving capability can be improved. Besides, only one closed-loop regulation is utilized to generate the charge pump circuit so as to improve the power conversion efficiency. By using this efficiency calculation the pumping efficiency also calculated and gets the detailed configuration of the proposed charge pump parameter evaluation. The degradation of the amplification could be highly reduces and it could be generated as per the test identification stages proposed in the charge pump design circuit. This circuit could be further used for the implementation of the like PLL based analog devices.

References

[1] C.Alippi and C.Galperti, "An adaptive system for optimal solar energy harvesting in wireless sensor network nodes," *IEEE Trans. CircuitsSyst.—I*, vol. 55, no. 6, pp. 1742–1750, Jul. 2008.
[2] C. Donovan, A. Dewan, H. Peng, D. Heo, and H. Beyenal, "Power management system for a 2.5W remote sensor powered by a sediment microbial fuel cell," *J. Power Source*, pp. 1171–1177, 2011.
[3] C. Donovan, A. Dewan, D. Heo, and H. Beyenal, "Batteryless, wireless sensor powered by a sediment microbial fuel cell," *Environmental Science and Technology*, vol. 42, no. 22, pp. 8591–8596, 2008.
[4] P. H. Chen *et al.*, "Startup techniques for 95 mV step-up converter by capacitor pass-on scheme and -tuned oscillator with fixed charge programming," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1252–1260, May 2012.
[5] E. J. Carlson *et al.*, "A 20 mV input boost converter with efficient digital control for thermoelectric energy harvesting," *IEEE J. Solid-StateCircuits*, vol. 45, no. 4, pp. 741–750, Apr. 2010.
[6] Y. O. Ramadass and A. P. Chandrakasan, "A battery-less thermoelectric energy harvesting interface circuit with 35 mV startup voltage," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 333–341, Jan. 2011.
[7] J. Hollemanet *al.*, "A compact pulse based charge pump in 0.13 m CMOS," in *Proc. IEEE Custom Int. Circuits Conf.*, 2007, pp. 381–384.
[8] A. Worapishet and J. B. Hughes, "Performance enhancement of switched-current techniques using sub threshold MOS operation," *IEEE Trans. Circuits Syst.—I*, vol. 55, no. 11, pp. 3582–3592, Dec. 2008.
[9] F. Pan and T. Samaddar, *Charge Pump Circuit Design*. NewYork: McGraw-Hill, 2006.
[10] *Jazz Semiconductor Design Application Manual*. Newport Beach, CA: Jazz Semiconductor Products Inc., 2012.
[11] J.-T. Wu and K.-L. Chang, "MOS charge pump for low voltage operation," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 592–597, Apr. 1998.
[12] L. Su and D.-S. Ma, "Design and optimization of integrated low-voltage low-power monolithic CMOS charge pumps," in *Proc.Int. Power Electron., Electrical Drives, Automation Motion*, 2008, pp. 43–48.
[13] F. Su andW.-H. Ki, "Gate control strategies for high efficiency charge pumps," in *Proc. Int. Symp. Circuits Syst.*, 2005, pp. 1907–1910.
[14] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Design of charge pump circuit with consideration of gate-oxide reliability in low-voltage CMOS process," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1100–1107,May 2006.
[15] B. Razavi, *Design of Analog CMOS Integrated Circuits*. NewYork: McGraw-Hill, 2001.

Author Profile

Ms. Juliet Abraham received her B.E in electronics and communication from Dr. Pauls engineering college, Pondicherry affiliated to Anna University, Chennai. Currently she is pursuing M.E in VLSI

Design from hindusthan institute of technology, Coimbatore, affiliated to Anna University, Chennai. Her area of interests is VLSI design and embedded system.

Dr. B. Paulchamy received his Ph.D. in Digital Signal Processing, Approach for De-Noising from EEG signal from Anna University Chennai, M.E degree in Applied Electronics from PSG College of Technology, Coimbatore, affiliated to Anna University Chennai, TamilNadu and B.E degree in Electronics and communication Engineering from National Engineering College, Kovilpatty, affiliated to Anna University Chennai, Tamilnadu. Currently he is working as Professor& Head in the department of ECE at Hindusthan Institute of Technology, Coimbatore. His research interests are Signal processing, Image processing and soft computing. He published around 15 papers in refereed conferences and journals. He is the Life Member in the Indian Society for Technical Education.