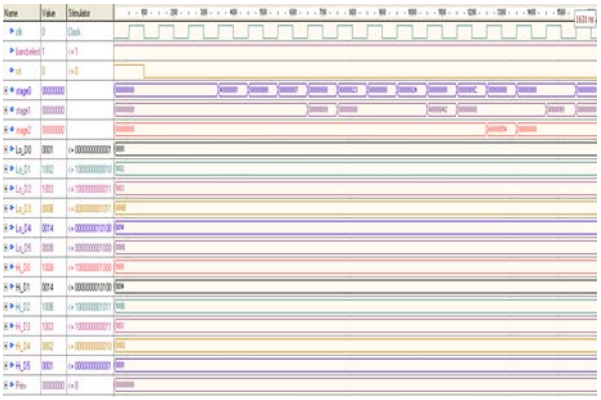

Figure 20: Simulated waveform of DWT-SA architecture for daubechies3 wavelet when band select is '0

Table 4 shows low pass coefficients and Table 5 shows high pass coefficients in hexadecimal form. Table 6 and Table 7 shows the result in terms of approximation coefficient and detail coefficients in hexadecimal form. Power analysis is shown in Table 8. and area analysis is shown in Table 9 . Clock speed for daubechies3 wavelet is 18. 69 MHz's.

Table 4: Low pass Coifficients of db3

Low pass coefficients	*Hex form*	*Binary form*
LO_D0	0001	0000000000001
LO_D1	1002	1000000000010
LO_D2	1003	1000000000011
LO_D3	000B	0000000001011
LO_D4	0014	0000000010100
LO_D5	0008	0000000001000

Table-5: High pass coifficients of db3

High pass coefficients	*Hex form*	*Binary form*
HO_D0	1008	1000000001000
HO_D1	0014	0000000010100
HO_D2	100B	1000000001011
HO_D3	1003	1000000000011
HO_D4	0002	0000000000010
HO_D5	0001	0000000000001

Table 6: Approximation Coefficients of db3

When band select is '1'		
Approximation coefficients of db3		
First stage output	*Second stage output*	*Third stage output*
ca1	ca11	ca111
-1	9	-54
7	-42	383
23	161	-6C9
24	51C	7AD8
1C	E0	700
0	0	0

Table 7: Details coefficients of db3

When band select is '0'		
Details coefficients of db3		
First stage output	*Second stage output*	*Third stage output*
cd1	cd11	cd111
C	100	1110
-2	05E	086E
1	0BA	114
-B	-1E	75
3	3	3
0	0	0

Table 8: Power Analysis for device EP2C20F484C7

Parameters	*Daubechies3*
Total Thermal Power Dissipation	257. 21mW
Dynamic Thermal power Dissipation	178. 74mW
Static Thermal Power Dissipation	47. 70mW
Input/output Thermal Power Dissipation	30. 78mW

Table 9: Area Analysis for device EP2C20F484C7

Parameters	*Daubechies3*
Total Logic Elements	1515, 8%
Total Combinational Functions	1320, 7%
Dedicated Logic Registers	336, 2%
LUT-only LCs	1179(1)
Register-Only LCs	195(0)
LUT/Register LCs	141(0)
DSP Elements	4
DSP 18×18	2

For the verification of VLSI results, MATLAB is used. The approximation and detail coefficient are obtained from MATLAB. Figure 21 shows the simulation waveform for approximation coefficients and Figure shows the simulation waveform for details coefficients for Daubechies3 wavelet.

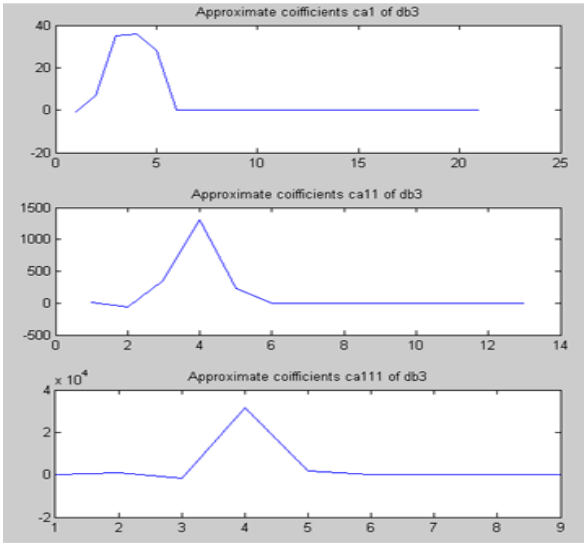

Figure 21: Simulation result of Approximation coefficients for Daubechies3

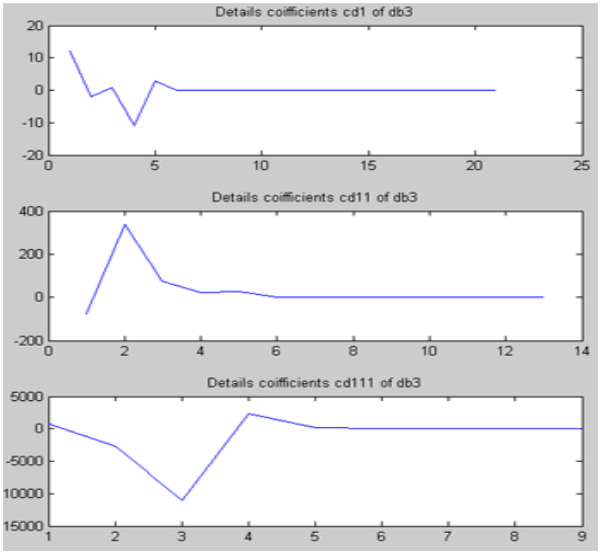

Figure 112: Simulation result of Details coefficients for Daubechies3

7. Conclusion

The main objective of this work is to develop a design resource for designers to implement systolic array architecture of DWT for Daubechies3 wavelet according to the design need such as clock speed, area and power. Systolic array architecture has efficient hardware utilization and it works with data streams of arbitrary size. The design is cascadable, for computation of one, two and three decomposition level. The real aim of our work is to decompose the data up to third level; proposed architecture is the best option. The total logic elements required for Daubechies3 is 8% respectively. This architecture does not use any external or internal memory modules to store the intermediate results and therefore avoids the delays caused by access, read, write and refresh timing.

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