3. Experimental Results

3.1 Result Analysis

Here test vectors generated by the LFSR with decoding circuit are given to the input of circuit under test and fault is detected by comparing the output of fault free circuit and faulty circuit by using comparator. The figures 6-10 are the simulation results done in the Xilinx ISE 12.1.The figure 9 shows no fault case in the s27 circuit and figure 10 shows there is a fault in the circuit. The clock and reset signals are inputs to the top level entity. If the comparator output is zero then no fault in the circuit else there is a fault in the circuit. Corresponding output waveforms are given below.

3.1 RTL Schematic

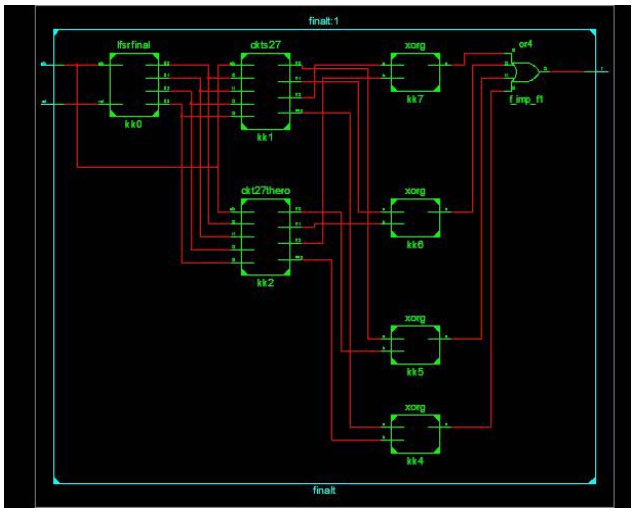

Figure 5: RTL Schematic

3.2 Output waveforms of LFSR

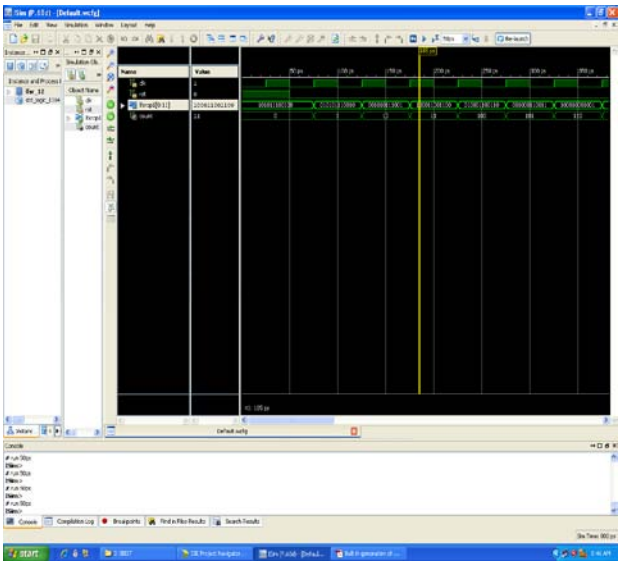

Figure 6: Output pattern at LFSR output

3.3 Generation of primary input sequence

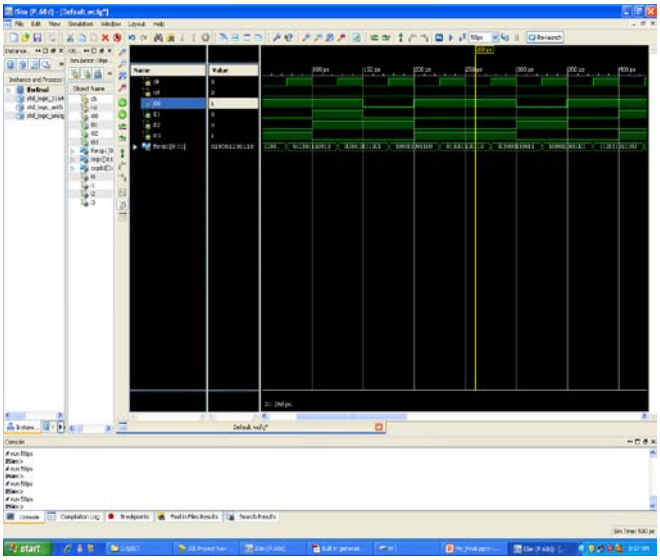

Figure 7: Generation of primary input sequence from the LFSR output

3.4 Output waveforms of s27 circuit

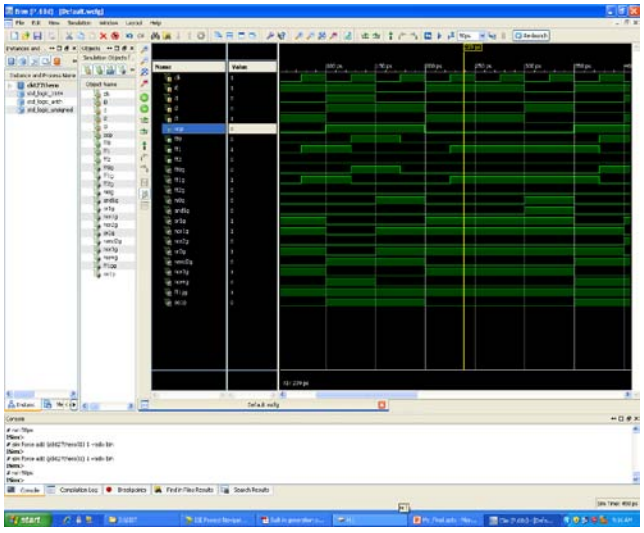

Figure 8: Output waveforms of s27 circuit

3.5 Waveforms represent no fault in the circuit

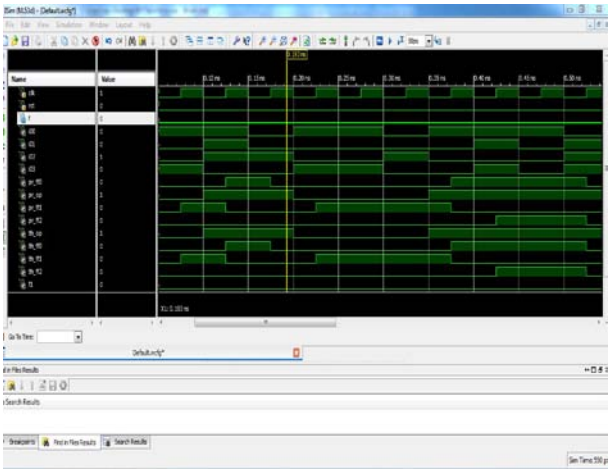

Figure 9: Waveforms represent no fault in the circuit

3.6 Waveforms represent fault in the circuit

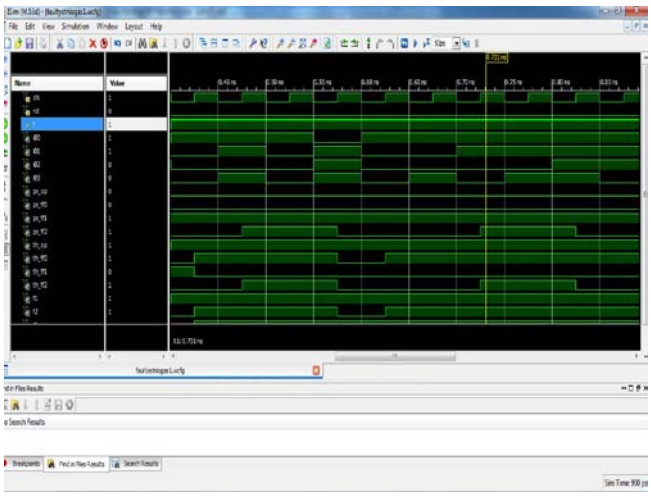

Figure 10: Waveforms represent fault in the circuit

4. Conclusion

The presence of delay-inducing defects is causing increasing concern in the semiconductor industry today. To test for such delay-inducing defects, on chip testing techniques are being implemented. On-chip test generation has the advantage it reduces test data volume, facilitates at-speed test application and achieves high fault coverage with low power estimated. The hardware used in this paper for generating the primary input sequence A consists of a linear-feedback shift-register (LFSR) as a random source and of a small number of gates to focus on reducing test pattern by avoiding repeated synchronization. The design is coded using VHDL language. The design is synthesized and simulated on Xilinx ISE 12.1 software.

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References

[1] J. Rearick, "Too much delay fault coverage is a bad thing," in Proc. Int. Test Conf., 2001, pp. 624–633.
[2] J. Saxena, K. M. Butler, V. B. Jayaram, S. Kundu, N. V. Arvind, P.Sreeprakash, and M. Hachinger, "A case study of IR-drop in structured at-speed testing," in Proc. Int. Test Conf., 2003, pp. 1098–1104.
[3] S. Sde-Paz and E. Salomon, "Frequency and power correlation between at-speed scan and functional tests," in Proc. Int. Test Conf., 2008, pp. 1–9, Paper 13.3.
[4] I. Pomeranz and S. M. Reddy, "Generation of functional broadside testsfor transition faults," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 25, no. 10, pp. 2207–2218, Oct. 2006.
[5] J. Savir and S. Patil, "Broad-side delay test," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 13, no. 8, pp. 1057–1064, Aug.1994.
[6] I. Pomeranz, "On the generation of scan-based test sets with reachable states for testing under functional operation conditions," in Proc. Design Autom. Conf., 2004, pp. 928–933.
[7] Y.-C. Lin, F. Lu, K. Yang, and K.-T. Cheng, "Constraint extraction for pseudo-functional scan-based delay testing," in Proc. Asia South Pacific Design Autom. Conf., 2005, pp. 166–171.
[8] Z. Zhang, S.M. Reddy, and I. Pomeranz, "On generating pseudo-functional delay fault tests for scan designs," in Proc. Int. Symp. Defect Fault Toler. VLSI Syst., 2005, pp. 398–405.
[9] I. Polian and F. Fujiwara, "Functional constraints vs. test compression in scan-based delay testing," in Proc. Design, Autom. Test Euro. Conf., 2006, pp. 1–6.
[10] M. Syal et al., "A study of implication based pseudo functional testing,"in Proc. Int. Test Conf., 2006, pp. 1–10.
[11] A. Jas, Y.-S. Chan, and Y.-S. Chang, "An approach to minimizing functional constraints," in Proc. Defect Fault Toler. VLSI Syst., 2006, pp.215–226.
[12] H. Lee, I. Pomeranz, and S. M. Reddy, "On complete functional broadside tests for transition faults," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., pp. 583–587, 2008.
[13] I. Pomeranz and S. M. Reddy, "On reset based functional broadside tests," in Proc. Design Autom. Test Euro. Conf., 2010, pp. 1438–1443.
[14] H. Lee, I. Pomeranz, and S.M. Reddy, "Scan BIST targeting transition faults using a Markov source," in Proc. Int. Symp. Quality Electron. Design, 2004, pp. 497–502.
[15] V. Gherman, H.-J. Wunderlich, J. Schloeffel, and M. Garbers, "Deterministic logic BIST for transition fault testing," in Proc. Euro. Test Symp., 2006, pp. 123–130.
[16] Y.-C. Lin, F. Lu, and K.-T. Cheng, "Pseudofunctional testing," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., pp. 1535–1546, 2006.
[17] M. Abramovici, M. A. Breuer, and A. D. Friedman, Digital Systems Testing and Testable Design. Piscataway, NJ: IEEE Press, 1995.
[18] I. Pomeranz and S. M. Reddy, "Primary input vectors to avoid in random test sequences for synchronous sequential circuits," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., pp. 193–197, 2008.
[19] I. Pomeranz, "Built-in generation of functional broadside tests," presented at the Design Autom. Test Euro. Conf., Grenoble, France, 2011.
[20] Built-In Generation Of Functional Broadside Tests Using A Fixed Hardware Structure Irith Pomeranz, Fellow, IEEE, Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 21, No. 1, January 2013.