

Figure 2: 3-2 compressor

This can be governed by the following equation

$$A + B + C = \text{Sum} + 2 * \text{Carry} \quad (1)$$

The architectures of traditional and enhanced version of 3-2 compressors along with sum and carry expressions are shown below.

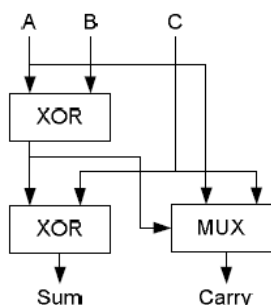


Figure 3: 3-2 Compressors Traditional architecture.

$$\text{Sum} = A \oplus B \oplus C \quad (2)$$

$$\text{Carry} = (A \oplus B) * C + \overline{(A \oplus B)} * A \quad (3)$$

**B. 4-2 Compressor**

The 4-2 compressor consists of 5 inputs A, B, C, D and Cin and will generate three outputs Sum, Carry, and Cout as shown in the figure 5.

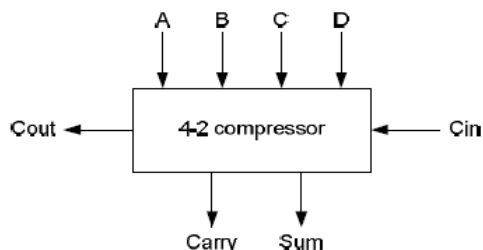


Figure 4: 4-2 compressor

In this the four inputs A, B, C, D and the output sum will have the same weight. The cin input is the output from a previous lower significant compressor and the output Cout is for the compressor in the next significant stage. The 4-2 compressor can be implemented with two full adders which are connected serially as shown in figure 6.

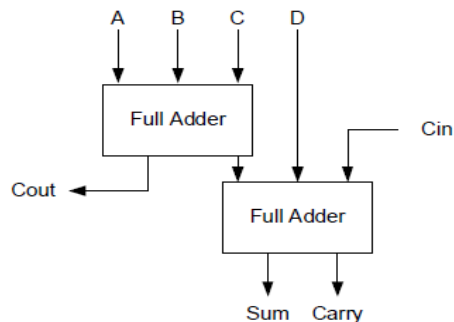


Figure 5: 4-2 Compressors with full adders

This can be governed by the following equation

$$A+B+C+D+Cin = \text{Sum}+2*(\text{Carry} +\text{Cout}) \quad (4)$$

The architectures of traditional and enhanced version of 4-2 compressors along with sum carry and Cout expressions are shown below.

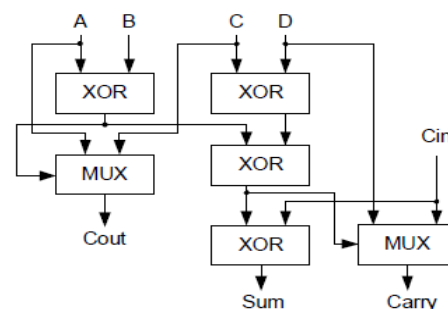


Figure 6: Traditional architecture of 4-2 compressor

$$\text{Sum} = A \oplus B \oplus C \oplus D \oplus Cin \quad (5)$$

$$\text{Cout} = (A \oplus B) * C + \overline{(A \oplus B)} * A \quad (6)$$

$$\text{Carry} = (A \oplus B \oplus C \oplus D) * Cin + \overline{(A \oplus B \oplus C \oplus D)} * D \quad (7)$$

**3. Design of Multiplier Using Compressors**

**3.1 Array Multiplier**

Multiplication is a mathematical operation; simply it is a process of adding an integer to itself in a specified number of times. The major steps involved in the multiplication are:

- Generation of partial product
- Reduction of partial product
- Final stage addition

In general case for the multiplication of an n-bit multiplicand with an m-bit multiplier, produce m number of partial products and the product is formed by n+m bits long. In order to perform N-bit/N-bit multiplication the N-bit multiplicand X is multiplied by N-bit multiplier Y to produce product Z. the unsigned binary numbers X and Y can be expressed as

$$X = \sum_{i=0}^n X_i 2^i \quad (8)$$

$$Y = \sum_{j=0}^n Y_j 2^j \quad (9)$$

The product of X and Y can be represented with Z and it can be written in the following form

$$Z = \sum_{i=0}^{n-1} \sum_{j=0}^{n-1} X_i Y_j 2^{i+j} \quad (10)$$

For the n\*n multiplier, n(n-1) adders and n<sup>2</sup> AND gates are required. In the case of simple array each row of 3-2 compressor will add a partial product to the partial sum which will generate a new partial sum and a sequence of carries. The delay of an array will depend on the depth of the array. Therefore the summing time of the simple array is N-2 of [3:2] compressors delay. Where N is the number of partial products.

### 3.2 8x8 Multiplier Design with 5:3 Compressors

The architecture of an 8x8 bit multiplier is shown in figure 9.

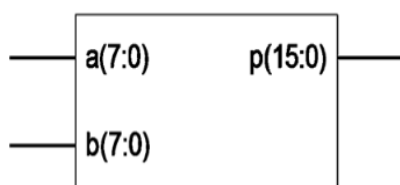


Figure 7: 8x8 bit multiplier

The Wallace tree architecture for an 8x8 bit multiplier is shown in fig 10. In this four stages are required to perform partial product. Different adders and compressors are used carefully to reduce the number of stages and to generate minimum number of outputs.

Now consider the column number four in figure 8, In which four bits are added at the first stage. These 4 bits could be added by using one full adder and it will produce two outputs. Instead of using this we proposed to use 4-2 compressor so that in the next stage we will have only 2 bits instead of 3 bits which in turns reduce the number of bits in the next stage. Now consider, column 5 in which five bits are added at the first stage. These 5 bits can be added with normal 3-2 compressors, it will produce 4 bits to the next stage of operation.

Instead of using normal compressors we propose traditional compressors which are designed with the combination of XOR gates and MUX circuits along with the binary counter property is contrasted with the conventional design. Using these high speed compressors we can reduce the vertical critical path which is independent of bit width, practically no area overhead when compared to carry propagate arrays (CPAs) on FPGAs.

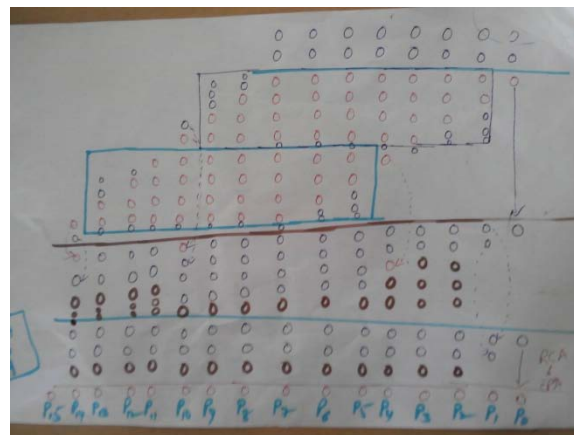


Figure 8: 8 bit multiplier with compressors

## 4. Performance Evaluation/ Results

The simulation results for an 8-bit multiplier in Xilinx ISE Simulator are shown in figure 9.

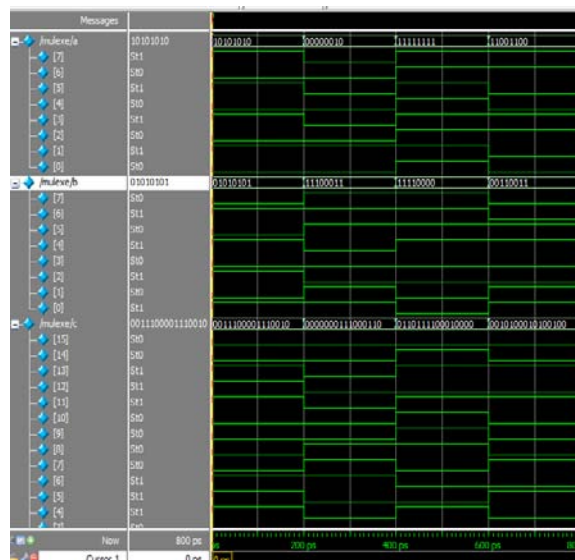


Figure 9: Simulated Waveforms

The RTL schematic for an 8-bit multiplier based on high speed compressors is shown in figure 10.

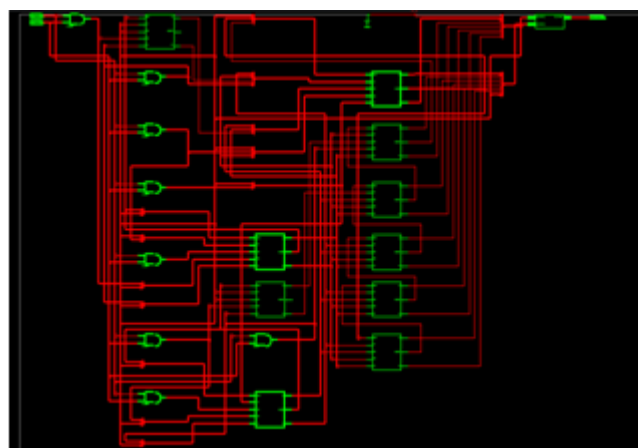


Figure 10: RTL Schematic

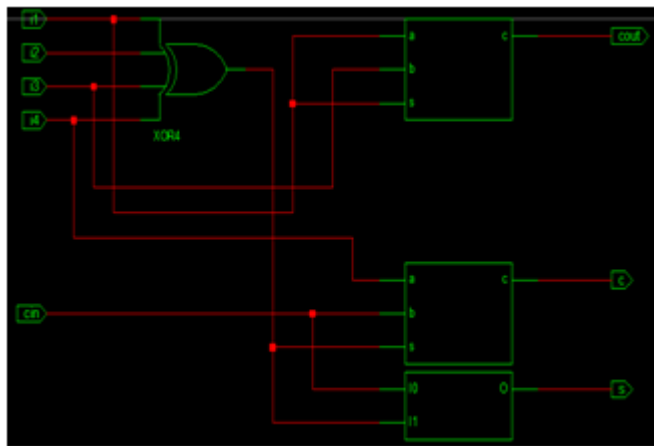


Figure 11: Multiplexer based Compressor Design

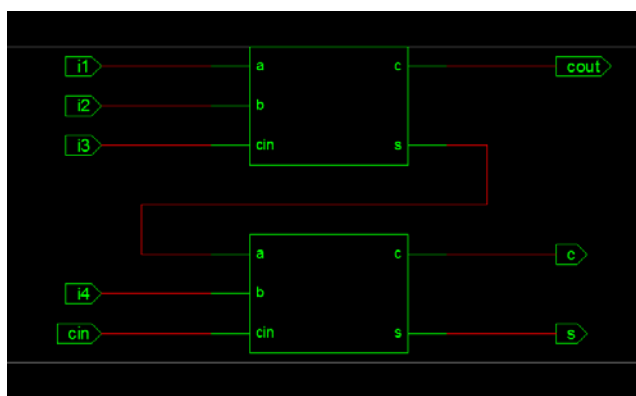


Figure 12: Traditional Compressor Design

As shown in the table 1 we summarize the different comparisons on power, delay, and power delay product (PDP), out of which the compressor based on Mux, produces low vertical Critical path delay results in reduction of power delay product.

Table 1: Power Comparison

S. No	Multiplier	Delay (ns)	Power (mw)	PDP (pws)
1	Array Multiplier	25.256	40	1010.2
2	Traditional Compressor	23.823	39	929.09
3	Mux based Compressor	21.63	40	865.48

As shown in the table 2 we summarize the comparisons on number of slices, and lookup tables (LUTs), out of which the compressor based on MUX, occupies less number of slices and LUTs which in turns reduces the area.

Table 2: Area Comparison

S. No	Multiplier	Slices used	Total slices	Used 4bit LUT's	Total LUT's
1	Array Multiplier	69	768	128	1536
2	Traditional Compressor	85	768	153	1536
3	MUX based Compressor	63	768	119	1536

### 5. Conclusion

In order to speed up the multiplication process different high speed compressors are used. Use of these high speed compressors in multipliers will simultaneously not only reduce the vertical critical path delay but also reduce the number of stage operations. By introducing the concept of high speed compressors on FPGA will reduce the no of slices, LUTs, PDP and increase the speed of operation by reducing the vertical critical path. Different comparisons are made in terms of Area, delay; Power and PDP are shown in the above Table1 and Table2

### 6. Future Scope

In order to perform higher order multiplications different compressors like 6-2, 7-2, and 9-2 compressors will help to reduce the area; power consumption and vertical critical path delay, and increases the speed of operation.

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